Novel Wafer-Scale Uniform Layer-by-Layer Etching Technology for Line Edge Roughness Reduction and Surface Flattening of 3D Ge Channels


Nanoelectronics Research Institute (NeRI)
AIST Japan
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What's oxygen etching?

Oxide Growth
Si + O₂ → SiO₂

Etching
2Si + O₂ → 2SiO↑
What's oxygen etching?

Low O\textsubscript{2} Pressure

High O\textsubscript{2} Pressure

Etching

Island Formation

What's oxygen etching?

What's oxygen etching?

Oxygen Etching of Si
$2\text{Si} + \text{O}_2 \rightarrow 2\text{SiO}$

Oxygen Etching of Ge
$2\text{Ge} + \text{O}_2 \rightarrow 2\text{GeO}$
Outline

• What's oxygen etching?
• Background
  – Why 3D Ge FET?
• Objective
• Measurement of O$_2$ Etching
• Electrical Characterization
• Discussion
• Summary
Background
Why 3D Ge FET?

3D channel

Buried oxide

Si

3-Dimensional transistor
(Fin or nanowire-FET)

Thin Channel → Off-Current Reduction

3D Si FET to 3D Ge FET
Issues in 3D Channel

- Plasma Damage Free
- Roughness Reduction
- Channel Slimming
Objective

• Can $O_2$ etching be applicable for nano-device fabrication?
Measurement of $O_2$ Etching
Surface Morphology

- Ge(001) AFM 2 × 2 μm

HF Treatment (Initial) → O₂ Etching

RMS 0.28 nm → RMS 0.12 nm

O₂ Etching \( P_{02} = 10^{-6} \) torr 640°C

Rough Step Edge Shape ➔ Etching of Step Edge
Etch Depth Measurement

• Mask Rebate Technique

Mask Patterning & Clean
Surface Formation

Wet-cleaned Ge or Si surface

SiO$_2$

Ge or Si

Etch depth

O$_2$ etching

Mask light etch & AFM

Visualization of Etch Depth

AFM after Mask Light Etch

Air View
0.5 x 0.5 μm

Etch depth
SiO₂ mask
Ge surface
Visualization of Etch Depth

AFM after Mask Light Etch

AFM Error Image
$5 \times 5 \, \mu m$

Etch Depth

SiO$_2$

Ge(001)
Visualization of Etch Depth

• Surface Cross-Sectional Profile

Etch Depth ~1 nm
Summary of Etch Rate

17 Ge

10^{-5} Si

10^{-6}

10^{-7}

PO₂ (Torr)

10^{-5}

10^{-6}

~1 nm/min

Etch rate (nm/min)

10^{-2}

10^{-1}

10^0

10^1

10^2

1/Temperature (10^{-4}/K)

950 900 840 800 720 640 500 (°C)
Summary of Etch Rate

- Weak Temperature Dependence
- Etch Rate $\propto$ O$_2$ Pressure
  - Supply of O$_2$ $\rightarrow$ Bottle-Neck Step
Comparison of Etch Rate Variation

**Ge**

Variation of Temp. ±5%

$E_A \sim 0.3 \text{ eV}$

Variation of Etch Rate (HCl)

Variation of Etch Rate (O$_2$)

$E_A \sim 0 \text{ eV}$

**HCl Etch:**

Uniform SOI Thinning

- Uniform Etching for Large Area
$O_2$ Etching of 3D Channel
Nanowire-FET by O$_2$ slimming

- SOI and hard mask formation -- (a)
- EB lithography & RIE -- (b)
- Cleaning
- O$_2$ Slimming -- (c)
- ALD HfO$_2$ & poly-Si gate
- NiSi$_2$ source/drain
- Dopant implantation & activation

SiNW direction: [110]
Nanowire-FET by O$_2$ slimming

Channel Cross-Section

Without O$_2$ Slimming

O$_2$ Slimming

50 nm-width SOI is etched from both sides.

$P_{O_2} = 1 \times 10^{-5}$ torr 900$^\circ$C

3.9 $\times$ 9.0 nm
LER Reduction

<table>
<thead>
<tr>
<th>Method</th>
<th>Ra (nm)</th>
<th>3σ (nm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>w/o O₂ etch</td>
<td>2.26</td>
<td>7.84</td>
</tr>
<tr>
<td>O₂ etch Ge</td>
<td>1.1</td>
<td>3.31</td>
</tr>
<tr>
<td>O₂ etch Si</td>
<td>0.52</td>
<td>1.94</td>
</tr>
</tbody>
</table>
I-V of O$_2$-Slimmed Si NW FET

- gate: NiSi$_2$
- source: NiSi$_2$
- drain: NiSi$_2$

$L_c \sim 360$ nm
$W_{NW} \sim 8$ nm

(a) $V_D = 0.05, 1$ V

(b) $V_G = 0-2$ V
(0.4 V step)
Discussion
Roughness Reduction

- Higher Temperature → Smaller Roughness

![Graph showing roughness reduction with different treatments.]

- Ge(001) w/o Anneal
- N₂ Anneal
- O₂ Etch

Etch Depth ~1 nm
Roughness Reduction

- O₂ etch can selectively reduce roughness.
  - AFM 2 × 2 μm

Ge(001) w/o anneal

O₂ Etching
PO₂ = 10⁻⁶ torr, 500°C
~ 1 nm Etching
RMS 0.14 nm

N₂ Anneal
PN₂ = 0.1 torr, 500°C
RMS 0.18 nm
Summary

• Novel $O_2$ Etching Technology for 3D Ge Channel
  – Uniform Etch Rate for Large Size Wafer
  – Atomically Flattened Surface
  – No Plasma Damage
  – Slimming and Smoothing for 3D Channels

• Enhancement of Device Performance

• Applicable for Future Channels
  – Vertical Nanowire
  – V-Groove etc..