ABSTRACT: The long term reliability of field deployed photovoltaic modules is dictated by four factors: (i) design quality, (ii) production quality, (iii) array/system configuration and (iv) actual combination of environmental conditions of the field. This paper discusses the design quality issues identified during the design qualification testing at ASU-PTL. The qualification testing does not, as anticipated, identify all the possible reliability issues in the actual field; however, it does identify the major/catastrophic design quality issues. ASU-PTL has been providing photovoltaic testing services since 1992 and has issued about 300 design qualification and type approval certificates. ASU-PTL received/continued its accreditation [per ISO17025 standard; formerly ISO Guide 25] in/since 1997 to provide testing services per IEC61215 (flat plate crystalline silicon), IEC61646 (flat plate thin film), IEEE1262 (flat plate crystalline silicon and thin film), UL 1703 (flat plate crystalline silicon and thin film) and IEEE1513 (concentrator) standards. These standards call for stress tests and non-stress tests before/after the stress tests. This paper presents an analysis on the design qualification test data, per IEC61215, IEC61646 and IEEE1262 standards, acquired between 1997 and 2005. During this period, about 1200 modules (87% c-Si and 13% thin-film technologies) have been subjected to over 8500 tests (including the performance tests). About 20% of these tests were stress tests and the other 80% were non-stress tests conducted before and after the stress tests. The results of all these tests were analyzed using, primarily, three approaches: (i) identify the percentage/order of failure rates for crystalline silicon technologies and thin-film technologies, (ii) identify the primary/potential reasons for these failures [viz. performance drop, major visual defect, dry/wet insulation breakdown], and (iii) finally, report the actual percent of power drop after the individual stress test. These data analyses indicate that the four of the highest failure rates, for c-Si technologies, were associated to damp-heat, thermal cycling (200 cycles), static load and bypass diode thermal stress tests. The primary reasons for failures in damp heat, thermal cycling static load and diode tests were performance drop beyond the maximum allowed limit of 5%, performance drop beyond the maximum allowed limit of 5%, module breakage and diode overheating beyond the maximum allowed junction temperature, respectively. The performance drop in damp heat and thermal cycling tests were primarily attributed to corrosion of cell components (due to moisture ingress) and differential thermal expansion of cell components (especially due to solder bonding and interconnect materials), respectively. The static load failure is attributed to inappropriate frame thickness, profile and/or design. The diode overheating was attributed to the use of underrated diodes. The highest failure rates, for thin-film technologies, were associated to damp-heat, outdoor exposure, static load and humidity-freeze stress tests. In conclusion, this investigation demonstrates that the accelerated stress tests used in the qualification testing and type approval programs do identify the major/potential design issues of photovoltaic modules. Keywords: Degradation, Performance, Qualification and Testing, Reliability

1 INTRODUCTION

The long term energy production (or reliability and durability) of photovoltaic modules in the actual field conditions is as critical as the initial performance/power under standard test conditions (STC) because the consumers essentially pay for the energy production over 20-30 years, not just for the initial power. The long term reliability of field deployed photovoltaic modules is dictated by four factors: (i) design quality, (ii) production quality, (iii) array/system configuration and (iv) actual combination of environmental conditions of the field. The module design quality is dictated by various parameters including the physical, chemical, electrical, optical and mechanical properties of cell/construction materials, cell and circuit design processes and packaging processes. The production quality is dictated by the material procurement control and process control including the workmanship related to manual soldering and junction box attachment. The array/system configuration such as the resistance of inadequate cable size and mounting methods also influence, to a notable extent, the reliability of the modules. The design qualified and production quality controlled modules could still fail, though to a very less extent, in the actual field as they may experience different combination/extent of environmental conditions.

This paper discusses the design quality issues identified during the design qualification testing at ASU-PTL. The design qualification testing is a set of well-defined accelerated stress tests [irradiation, environmental, mechanical and electrical] with strict pass/fail criteria. The type, extent, limits and combination of these accelerated stress tests have been stipulated with two goals in mind: (i) accelerate the same failure mechanisms observed in the field without causing failures that do not occur in the filed, and (ii) induce these failure mechanisms in a reasonably short amount of time, say 70-120 days. The qualification testing does not, as anticipated, identify all the possible reliability issues in the actual field; however, it does identify the major/potential design quality issues. ASU-PTL has been providing photovoltaic testing services since 1992 and has issued about 300 design qualification and type approval certificates. These design qualification tests (and the corresponding type approval certificates) are
used by consumers for procurement specifications (along with supplier/manufacturer warranty) and by manufacturers for demonstrating as a potential measure of product reliability. ASU-PTL received/continued its accreditation [per ISO17025 standard; formerly ISO Guide 25] in/since 1997 to provide testing services per IEC61215 (flat plate crystalline silicon), IEC61646 (flat plate thin film), IEEET262 (flat plate crystalline silicon and thin film) and IEEET2153 (concentrator) standards. These standards call for stress tests and non-stress tests before/after the stress tests. Excellent studies related accelerated qualification testing for crystalline silicon technologies per IEC61215 standard, accelerated reliability testing (for example, a prolonged accelerated stress testing until the failures are induced) for crystalline silicon technologies and accelerated reliability testing for thin-film technologies are already presented. This paper presents an analysis on the design qualification test data for both crystalline silicon and thin-film technologies (per IEC61215, IEEET2646 and IEEET262 standards) acquired by ASU-PTL between 1997 and 2005.

2 METHODOLOGY

During the 9-year period between 1997 and 2005, about 1200 modules have been subjected to over 8500 tests (including the performance tests). About 20% of these tests were stress tests and the other 80% were non-stress tests that are conducted before and after the stress tests. The results of all these tests were analyzed using, primarily, three approaches: (i) identify the percentage/order of failure rates for crystalline silicon technologies and thin-film technologies, (ii) identify the primary/potential reasons for these failures [viz. performance drop, major visual defect, dry/wet insulation breakdown], and (iii) finally, report the actual percent of power drop after the individual stress test.

3 RESULTS AND DISCUSSION

Figure 1 presents the total number of modules of all the technologies subjected to each of the stress and non-stress tests between 1997 and 2005. The data presented in Figure 2, for c-Si, indicates that the four of the highest failure rates for c-Si technologies were associated to damp-heat, thermal cycling (200 cycles), static load and bypass diode thermal stress tests. The primary reasons for failures in damp heat, thermal cycling, static load and diode tests were performance drop beyond the maximum allowed limit of 5%, performance drop beyond the maximum allowed limit of 5% and performance drop beyond the maximum allowed limit of 5% or, module breakage and diode overheating beyond the maximum allowed junction temperature, respectively. For the thin-film technologies, the highest four failure rates were associated to damp-heat, outdoor exposure, static load, and humidity freeze tests. The performance drop in damp heat/humidity freeze and thermal cycling tests were primarily attributed to the corrosion of cell components (due to moisture ingress) and differential thermal expansion of cell components (especially due to solder bonding and interconnect materials), respectively. The static load failure was primarily attributed to frame design, thickness and profile. The diode overheating was attributed to the use of inadequate diodes. The outdoor exposure test failure of thin-film technologies was primarily attributed to Staebler-Wronski effect of amorphous silicon technologies. Majority of the post-test (predominantly post-chamber test) wet insulation failures shown in Figure 2 and Figure 3 are traceable to the junction box area, especially to the interface between backsun and junction-box of the modules. Figure 4 quantifies whether a particular stress test failure (for all technologies) is related to the performance or non-performance (visual, dry and/or wet insulation) issue.

As shown in Figure 5, some modules (both c-Si and thin-film technologies) experienced catastrophic failures during the damp-heat test with more than 10% power loss indicating a severe design issue related moisture ingress leading to chemical corrosion and altering cell properties. The slight power gain (less than 4%) shown in Figure 5 is attributed either to insufficient out-of-the-box light conditioning/exposure of crystalline silicon technologies before the initiation of the damp heat test or to the annealing effects of amorphous silicon technologies. The current version of IEC61215 (edition 2 released in April 2005) addresses this insufficient light conditioning issue by introducing a pre-test 5 kWh light conditioning of all the crystalline silicon modules destined for the design qualification and type approval programs. The huge power gain (as high as 22%) shown in figure 5 is attributed to the annealing effects of some of the amorphous silicon technologies.

4 CONCLUSIONS

Highest failure rates in the qualification testing programs are associated to the post-chamber performance and wet insulation tests. Significant failure rates are associated to bypass diode, termination, outdoor exposure and static load tests. Recognizing that there are about 15 stress tests involved in a typical design qualification testing program and even a single test failure will nullify the whole test program, these individual test failure rates still need to be reduced to produce reliable photovoltaic modules and receive successful type approval certifications.
Figure 1: Number of stress and non-stress tests (excluding performance tests) conducted at ASU-PTL between 1997 and 2005.

Figure 2: Failure rates of stress and non-stress tests for c-Si technologies conducted at ASU-PTL between 1997 and 2005.

Figure 3: Failure rates of stress and non-stress tests for Thin-Film technologies conducted at ASU-PTL between 1997 and 2005.

Figure 4: Failure rates of stress tests conducted at ASU-PTL between 1997 and 2005, (all the technologies).

Figure 5: Power drop after damp heat test conducted on all technologies at ASU-PTL between 1997 and 2005.

5 REFERENCES


