Low-Voltage Wide-Dynamic Range CMOS Log Domain Filter Using Companding Technique

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Abstract

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This dissertation proposes novel design techniques of low-voltage CMOS analog filters with wide dynamic range through the companding techniques. First, it is pointed out that an instantaneous companding integrator, which is a building block of continuous-time filters, has a degree of freedom to configure its topology, and then a synthesis method of all the integrators is proposed. Synthesized 45 integrators including known four ones are compared to each other by simulations, and some intrinsic features of each topology are found from the results. Two 1.0-V 2nd-order Butterworth low-pass filters fabricated in a 0.35-μm CMOS technology as an application example of the integrators are also compared through its measured results. Furthermore, a selection of log domain integrator cores from the integrators is discussed for higher-order log domain filter design.

One of the selected log domain filter cores is used for syllabic companding filters the internal voltage swings of which are dynamically amplified as large as possible by sensing an input or an output signal of the filters. Combining log domain circuits with the syllabic companding technique, filters are easily implemented by use of one transistor as an amplifier, in which these filters are also called as dynamically adjustable biasing (DAB) ones because a gain of the amplifier is set by a dynamic bias current. Although a conventional DAB-based filter requires a supply voltage of 2.5 V, filters based on a modified DAB technique can operate at lower-supply voltages,

0.8 and 0.6 V, with keeping wide-dynamic range. Two 5th-order Chebychev low-pass filters are designed to confirm effectiveness of the proposed technique. The one is fabricated in a 0.35-μm CMOS technology and the other is done in a 0.18-μm one. The former achieves a 78-dB dynamic range at a power supply of 0.8 V. On the other hand the latter filter has a dynamic range of 89 dB and consumes 443 μW, and then the filter is compared to other recently published filters through a figure of merit (FOM) which is calculated by use of dynamic range, bandwidth, filter order, and power consumption. The filter achieves an FOM of 3.83 fJ from a power supply of 0.6 V, which represents effectiveness of the proposed scheme in the view of a trade-off between a supply voltage and a dynamic range.

To design the filters with wider dynamic range in a short time, an optimum design method is presented. The method uses a signal-to-noise-plus-distortion ratio as an evaluation function from an analyzed noise characteristic and a distortion model. The method does not need any transient simulations, reducing the simulation time: a reduction of about 1/48 is achieved. Furthermore low-voltage biasing circuits, such as control circuits, a voltage reference circuit, and a frequency tuning system, are also proposed for higher performance and integration. The control circuits, which provide a dynamic bias current, include a low-voltage current peak detector and measured results of its prototype chip in a 0.35-μm CMOS process shows a wide-detection range from a 0.8-V supply. To achieve low-voltage operation a voltage reference circuit uses p-channel MOSFETs in weak inversion region instead of bipolar transistors in conventional bandgap reference circuits. The simulated results show a temperature coefficient of -25.5 ppm/C$^\circ$ at 27 C$^\circ$. The fabricated reference circuit in a 0.18-μm CMOS technology outputs a voltage of 0.4 V from a 0.55-V power supply at a room temperature. The frequency tuning system based on a voltage-controlled filter is proposed by replacing a high-gain amplifier with a duty ratio detector and a charge pump circuit for low-voltage operation. Stability analysis of the system is also described.

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Chapter 1

General Introduction

1.1   Background and Motivation

Analog circuits are required as an interface between physical quantities, such as sounds or electromagnetic waves, and a digital code described as "0" or "1," which is processed by a computer and gives us information. For a lower cost of the devices analog and digital circuits have been integrated together on a complementary metal-oxide semiconductor (CMOS) chip. Furthermore, a CMOS technology scaling which means to shrink the width of the metal line and the gate length of the transistor has helped to reduce power consumption, cost, and size and to push more integration and high-speed operation in digital circuits.

The CMOS technology scaling requires new low-supply voltage design techniques for analog integrated circuits (ICs) because of a degradation of the device breakdown voltage and a demand of low-power consumption. The International Technology Roadmap for Semiconductors (ITRS) shows the prospects of relation between technology node and power-supply voltage V_{DD} for the future as shown in Fig. 1.1 [1]. In this figure it is clearly confirmed that the shorter the width of the metal line in ICs is, the lower the supply voltage becomes. Nevertheless, a threshold voltage V_{th} of a transistor cannot be decreased like the supply voltage in digital circuits because a subthreshold leak current, which arises even as a transistor is switched off, must be suppressed. In an analog circuit design a transistor the gate-to-source voltage of which is set above V_{th} is generally used to obtain a large gain. Therefore what V_{th}
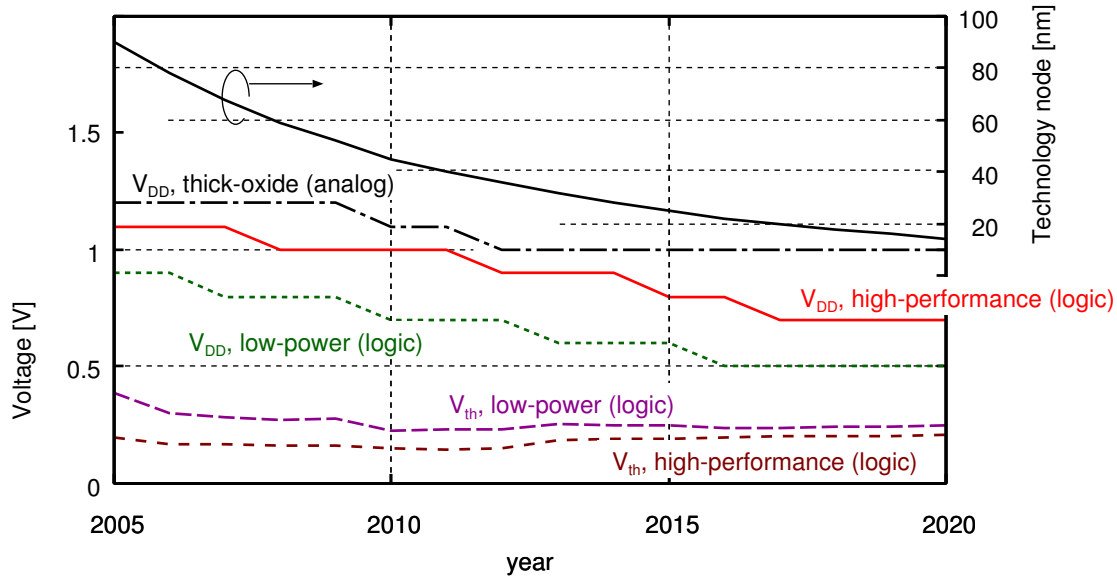
Figure 1.1: Technology road map for semiconductor in the future: relation among technology node, supply voltage V_{DD}, and threshold voltage V_{th} [1].

does not reduce in comparison to V_{DD} makes it difficult to design analog circuits with a sub-micron CMOS process. There are some solutions for the above problem in analog circuit designs: using a thick oxide in a gate of a transistor [2], [3] and low-V_{th} devices [4]–[6] which increase cost for additional masks. Another is to utilize several low-voltage analog circuit design techniques described in Refs. [3], [7]–[11], especially, log domain circuit design technique [12] which employs non-linearity of a transistor for linear signal processing. By use of these techniques, amplifiers [5], [13]–[15] and filters [16]–[21] under 1.0-V supply have been developed in the past several years.

In addition to the issue about lower supply voltage a dynamic range (DR) of analog circuits must be considered. Since low-supply voltage makes a signal swing in analog circuits degraded while a noise level is not decreased, its DR reduces. In general for the sake of enhancing DR an auto gain controlled (AGC) circuit is utilized in front of a filter [22]. In an AGC circuit a variable gain amplifier (VGA) the gain of which is appropriately adjusted amplifies an input signal to obtain wide DR at the output. Other techniques are described in Ref. [23]: the impedance scaling and the companding technique. The companding technique is suitable for realizing a wide DR

signal processor [23], [24]. Voltage swing of internal node of a companding circuit is almost constant and a constant signal-to-noise ratio (SNR) over wide DR is brought. Especially, the dynamically adjustable biasing (DAB) technique, which is combination of the companding technique and a log domain circuit, is attractive because amplifiers on a DAB circuit are easily implemented by use of only one transistor [25], [26]. However, conventional circuits using these techniques require a power supply of 1.2 V to 3.3 V. Therefore a design technique to alleviate a trade-off between supply voltage and DR is required in any applications, for example a sub-1V filter with more than 80-dB DR which is a GSM (global system for mobile) specification.

1.2   Overview of the Dissertation

This dissertation describes design techniques of low-voltage wide DR log domain filter using the DAB technique and shows measured results of prototype chips.

In Chapter 2 a conventional low-voltage operational transconductance amplifier (OTA), a filter as its application example, and several conventional techniques for wide dynamic range are reviewed. Furthermore the two classified companding techniques, instantaneous and syllabic types, are also introduced. Chapter 3 shows a synthesis method of all low-voltage instantaneous companding log domain integrators. The method clarified unknown topologies of the integrators and two instantaneous companding filters as its application example are compared through measured results. A selection of a building block is also discussed for the later Chapters in the view of higher-order filter synthesis. In Chapter 4 a low-voltage syllabic companding technique is proposed by modifying the conventional DAB technique and then an integrator and filters are designed. A control current dynamically adjusts an appropriate operating point of the circuits for low-voltage operation and wide DR. An externally linear and time invariant (ELTI) relation between an input and an output of the circuits is endured by use of new state variable correction (SVC) methods. Chapter 5 shows an optimum design method of the control current for wider DR by using DC characteristics of a low-voltage DAB-based filter and the analyzed noise

expression. Since the method does not need any transient simulation, a short design time is expected. In Chapter 6 a low-voltage frequency tuning system, a voltage reference circuit, and a control circuit are described. These biasing circuits are applicable to any low-voltage log domain filters. Measured results of prototype filter chips of proposed filters are shown in Chapter 7. One of the filters is compared to the other recently published filters through a figure of merit (FOM) which is calculated from DR, bandwidth, filter order, and power consumption. Finally, Chapter 8 concludes the dissertation and the future works are given.

Chapter 2

Review of Conventional Filters

2.1   Low-Voltage Filters

An active integrated filter is composed of passive components, such as resistors
and capacitors, and operational amplifiers or operational transconductance amplifiers
(OTAs) as active components by transforming an RLC prototype ladder filter into
a structure using integrators [27]–[29]. These amplifiers require a power supply, and
then a differential amplifier shown in Fig. 2.1 (a) is generally employed [30],[31] where
a common-mode feed back (CMFB) circuit makes a common-mode output voltage
$V_{DD}/2$ and its circuitry is omitted. In this figure a required minimum supply voltage
is considered. In order that a MOSFET M_0 as a tail current source is biased in
saturation region, its drain-to-source voltage must be larger than $V_{ds,sat}$. A gate-
to-source voltage of M_{a1} and M_{a2} requires $V_{gs,a}$ which corresponds to the overdrive
voltage $V_{ov,a}$ plus the threshold voltage V_{th} of the MOSFETs, and thus a common-
mode input voltage needs a voltage of $V_{ds,sat} + V_{ov,a} + V_{th}$, which equals at least 0.9
V in a standard 0.18-μm CMOS process where $V_{ds,sat} = 0.2$ V, $V_{ov,a} = 0.2$ V, and
$V_{th} = 0.5$ V. In general since a common-mode input voltage is set as a half of a
supply voltage V_{DD}, V_{DD} must be larger than 1.8 V. In this case it is assumed that
potentials of the output are minimum, or $V_{ds,sat} + V_{ov,a}$, and thus an output voltage
can swing from 0.4 to 1.6 V.

Recently, an OTA with a power supply of 0.5 V and a filter as its application
example have been presented in Refs. [15]–[17]. The circuitry of the OTA is shown
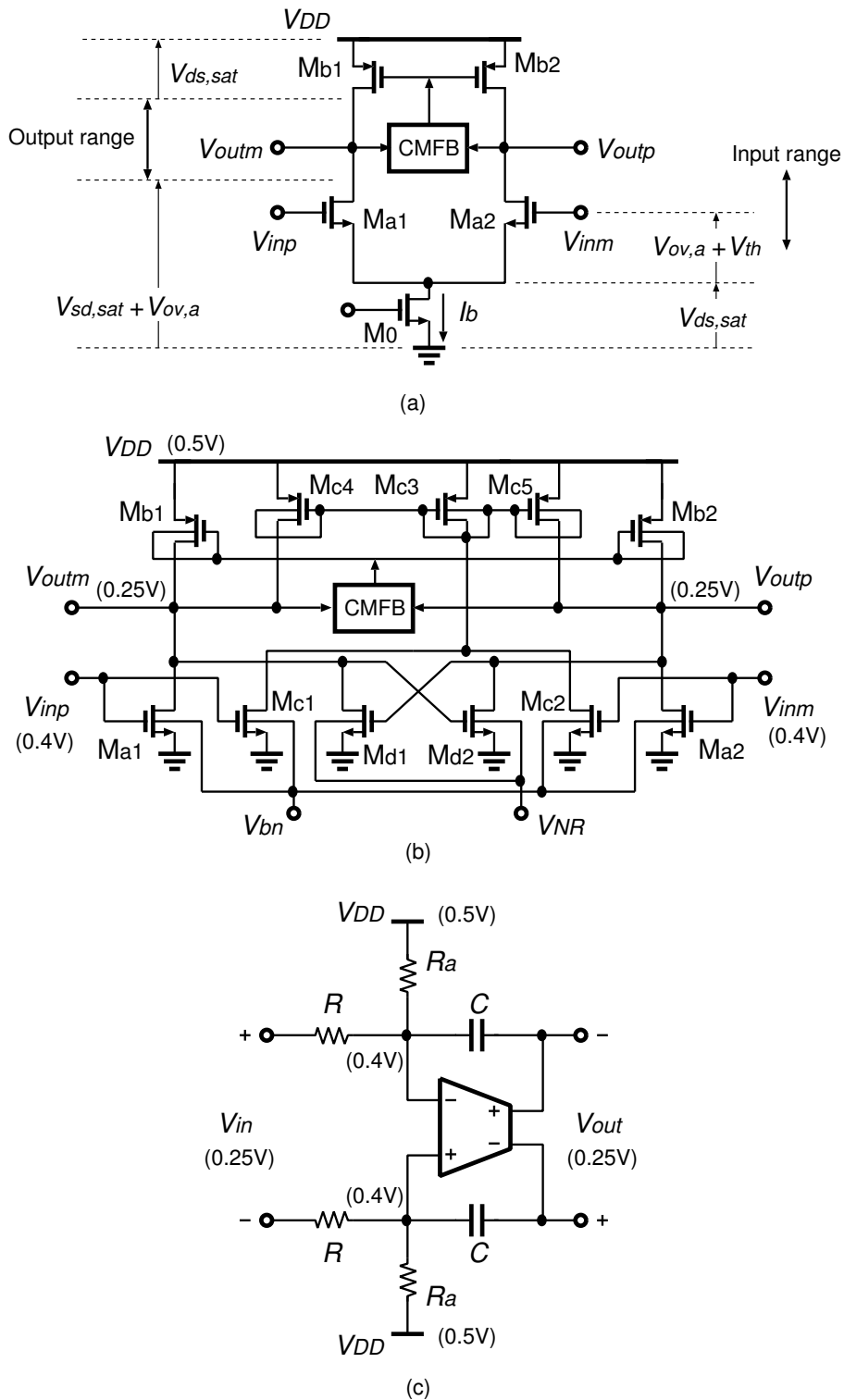
Figure 2.1: Operational transconductance amplifiers (OTAs) and an integrator: (a) a conventional differential amplifier as OTA, (b) a 0.5-V OTA, and (c) a 0.5-V integrator [16].
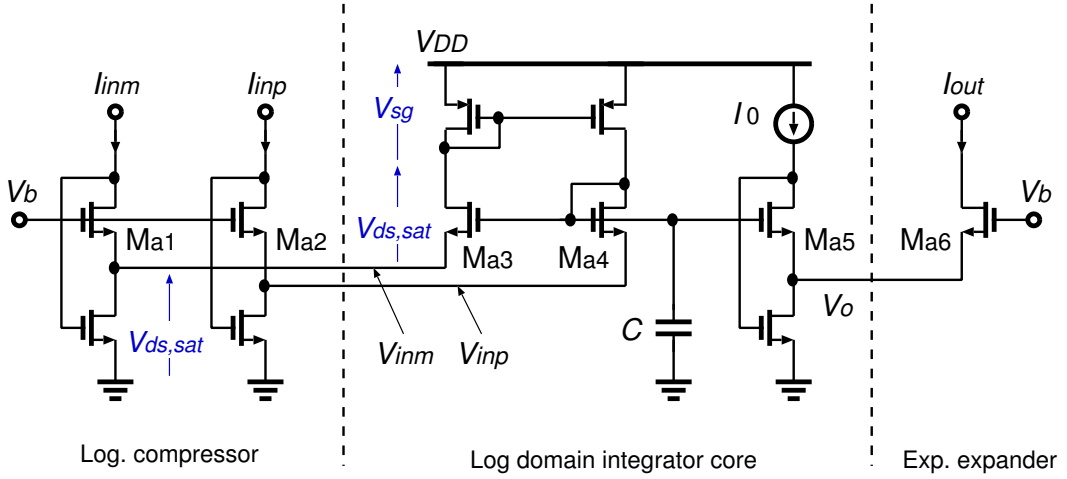
Figure 2.2: Low-voltage CMOS log domain integrator [33].

in Fig. 2.1 (b). In this figure a tail current source is removed out, while MOSFETs M_{ci} ($i = 1$ to 5) are added for a common-mode rejection. For enhancing DC gain of the OTA the MOSFETs M_{c1} and M_{c2} as a negative resistor are used where its value is automatically controlled by V_{NR}. The common-mode output voltage is $V_{DD}/2 = 0.25$ V, while the common-mode input voltage is set as 0.4 V to bias the input devices, M_{a1}, M_{a2}, M_{c1}, and M_{c2}, in a moderate inversion region. An integrator for a filter is therefore configured as shown in Fig. 2.1 (c) where a resistor R_a is used to set a common-mode input voltage into 0.4 V. A 5th-order elliptic low-pass filter with 135-kHz cutoff has been implemented by use of the 0.5-V integrators in a 0.18-μm CMOS with triple well process and the measured results show the filter has dynamic range of 57 dB [16].

A log domain circuit is also usable for low-voltage analog filter design [12]. Log domain circuits use an exponential function of a bipolar transistor for linear signal processing [12], [32]–[36]. Since a MOSFET in weak inversion region, which means $V_{gs} < V_{th}$, also expresses the function, log domain circuits composed of such MOSFETs have been reported in Refs. [18], [37]–[42]. Figure 2.2 shows a CMOS log domain integrator as an example circuity [33]. A differential input current $I_{inp} - I_{inm}$ and an output current I_{out} have a relation of linear integrator, while internal node voltages behave as a logarithmic manner for the input and the output currents. In

this figure differential input currents, I_{inp} and I_{inm}, are logarithmically compressed and converted into voltages, V_{inp} and V_{inm}. The voltages are processed in log domain by a log domain integrator core, which outputs a voltage V_o. An output current I_{out} is obtained by an exponential function of a MOSFET M$_{a6}$. A required supply voltage V_{DD} is equal to $V_{sg} + 2V_{ds,sat}$, which is about 0.6 V for a 0.18-μm CMOS technology and 0.8 V for a 0.35-μm one. Log domain filters are also implemented by use of floating-gate MOS (FGMOS) transistor, and then the filters can operate under 1.0-V supply [43], [44]. Measured results of these conventional log domain filters below a power supply of 1.0 V show that its dynamic ranges are around 60 dB [41]–[43]. All-pole higher-oder log domain filters are synthesized by use of log domain integrator cores as shown in Fig. 2.2 [45]–[48]. Another technique using non linearity of a MOSFET is the squire-root-domain one, which is difficult to achieve a low-voltage operation because its transistors are biased in strong inversion region, $V_{gs} > V_{th}$ [49]–[52].

2.2   Wide-Dynamic Range Techniques

Signal-to-noise-plus-distortion ratio (SNDR) and dynamic range (DR) are important characteristics of continuous-time filters. If an input signal, an output noise, and a distortion component are denoted as V_s, V_n, and V_d, respectively, then SNDR is expressed as

$$\text{SNDR} = 10\log\frac{V_s^2}{V_n^2 + V_d^2} \ [\text{dB}] \tag{2.1}$$

where filter with a 0-dB passband gain is assumed [23], [24]. In general a noise is dominant for SNDR at a small input signal, while a distortion is so at a large input in continuous-time filters as shown in Fig. 2.3. On the other hand, DR is defined as

$$\text{DR} = 20\log\frac{V_{s,max}}{V_n} \ [\text{dB}] \tag{2.2}$$

where $V_{s,max}$ is generally an input signal under -40-dB total harmonic distortion (THD) at the output [16], [26]. If wider DR is required, one should reduce V_n or
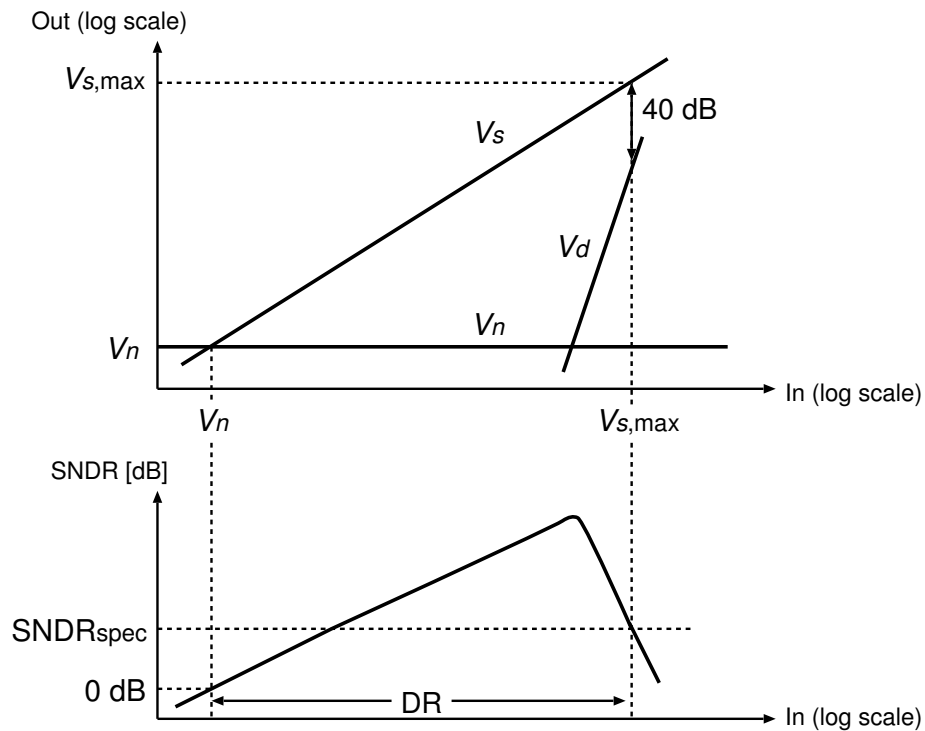
Figure 2.3: Relation between signal-to-noise-plus-distortion ratio (SNDR) and dynamic range (DR).
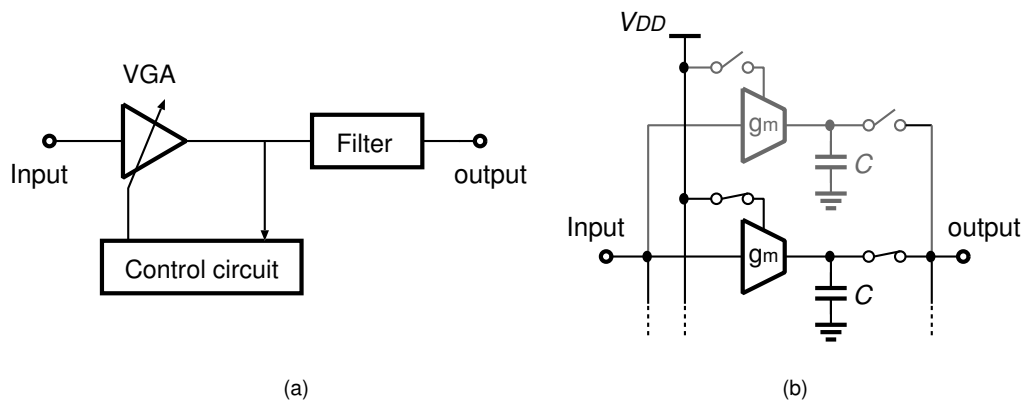
Figure 2.4: Techniques for wide-dynamic range analog signal processing: (a) a filter with an automatic gain controlled (AGC) circuit and (b) an integrator in a filter using dynamic impedance scaling technique.

increase $V_{s,max}$ which means decreasing a distortion V_d of filters. However, it is difficult to obtain a large signal swing under low-supply voltage.

One of solutions for the issue is to use an auto gain controlled (AGC) circuit in
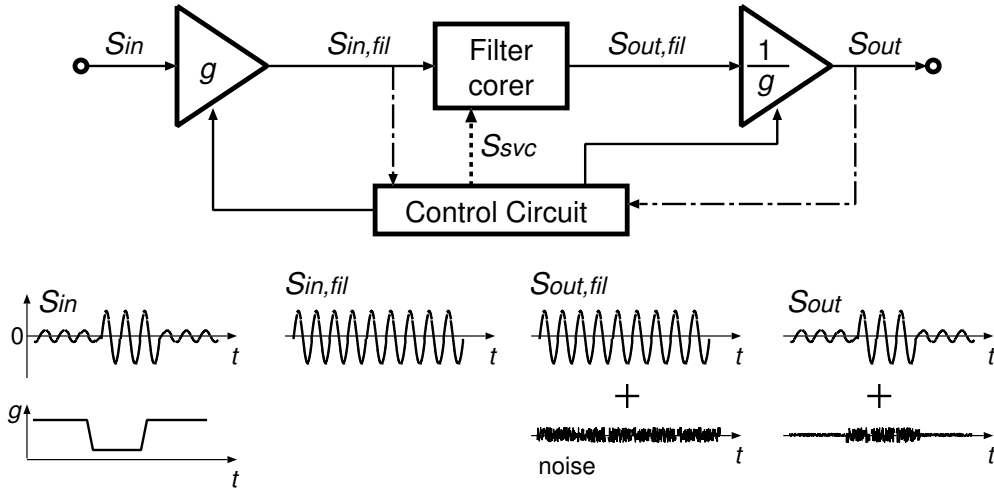
Figure 2.5: A filter using the companding technique and its conceptual waveforms.

front of a filter as shown in Fig. 2.4 (a) [22]. In a variable gain amplifier (VGA) its gain is set by a control circuit to keep an input signal swing of the filter as large as possible without a distortion from the filter. Therefore DR at an output of the filter is extended where it is assumed that a noise of the VGA is ignored. On the other hand, there is a method that reduces a noise V_n in Eq. (2.2) to extend DR. In general an output noise of a filter is proportional to kT/C where k is Boltzmann constant, T is absolute temperature, and C is a capacitance of integrator in the filter [23], [31]. Hence, the noise of the filter is inversely proportional to capacitance C. For example, if a small noise for a small input signal at the integrator is required, then an additional integrator is dynamically connected in parallel to increase capacitance C as shown in Fig. 2.4 (b), which called as the dynamic impedance scaling technique [23], [53], [54]. In this figure since a transconductance g_m of the OTAs and a capacitance C must be simultaneously scaled up or down to keep a unity gain angular frequency g_m/C of the integrator constant where the OTA in the unused path is turned off for lower power consumption. The filter based on the dynamic impedance scaling technique has achieved 80-dB DR at a power supply of 1.2 V [54].

The companding, which is a coined word from compressing and expanding, is also one of techniques to enhance DR [23]–[26], [55]–[62]. A companding filter and
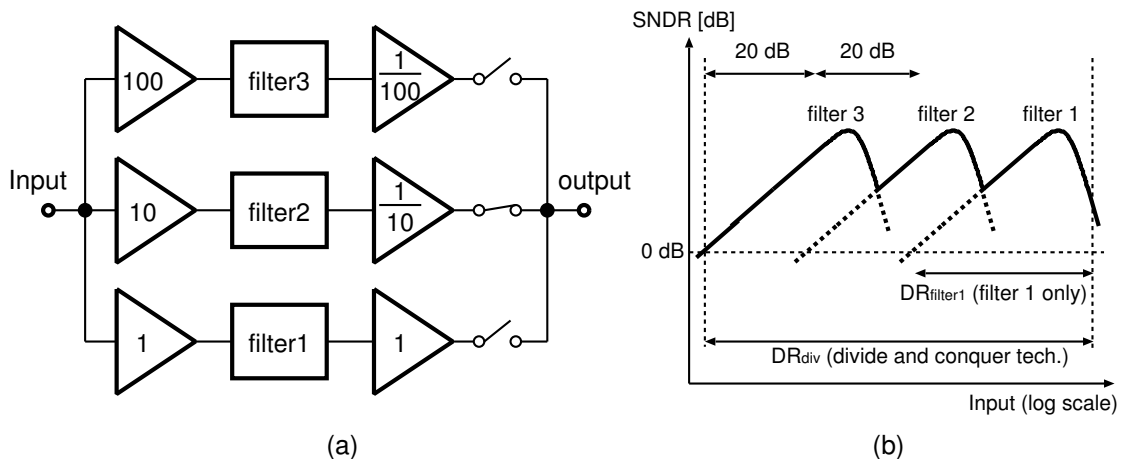
Figure 2.6: Divide-and-conquer technique: (a) the block diagram and (b) its signal-to-noise-plus-distortion ratio (SNDR).

its conceptual waveforms are shown in Fig. 2.5 where two VGAs with gains of g and $1/g$ are located in front of and behind a filter core. A control circuit detects an envelope of an input of the filter core $S_{in,fil}$, an input S_{in}, or an output S_{out} of the companding filter, making g an appropriate value in order to suppress an output noise or distortion. The circuitry and the behavior of the companding filter are similar to a filter with AGC circuit in Fig. 2.4 (a) except for a VGA at the output stage. A most important feature of companding filter is to maintain an externally linear and time invariant (ELTI) relation between the input S_{in} and the output S_{out} even if gains of VGAs changes dynamically during signal processing [23], [24]. The ELTI relation is guaranteed by use of a state variable correction (SVC) circuit in a control circuit, and then a signal for SVC is denoted as S_{svc} in Fig. 2.5. If there is no SVC signal S_{svc}, a change of the gain of VGAs results in a disturbance for the output S_{out}.

A practical implementation of companding filters is shown in Fig. 2.6 (a), which is called as the divide-and-conquer technique [61], [62]. In this figure three paths including two amplifiers with a different fixed gain and the same filter for each are used, and then one of the paths is dynamically selected during signal processing. The selection is determined by detecting an output signal strength of the middle path: filter 2 in Fig. 2.6. For example, if the output signal is large, the lowest path with
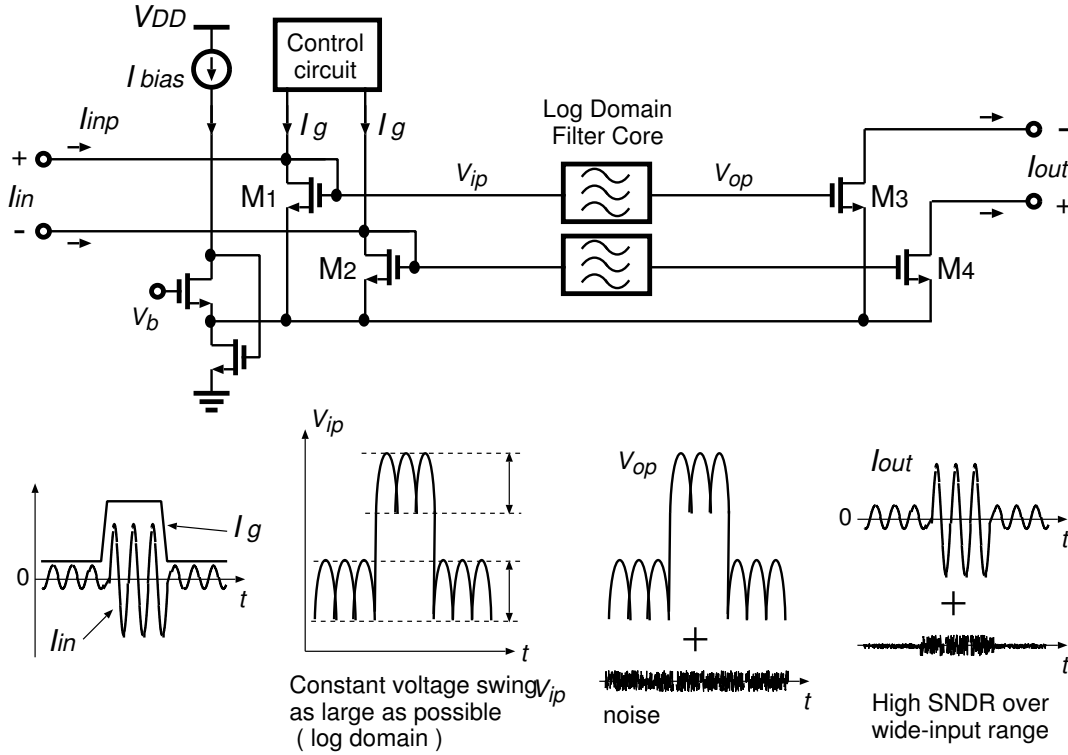
Figure 2.7: A filter using the dynamically adjustable biasing (DAB) technique and its conceptual waveforms.

filter 1 is selected for distortion immunity. On the other hand, the topmost path is switched on for the small output in order to reduce an output noise. Therefore if the gains of amplifiers for each path are set like as shown in Fig. 2.6 (a), the SNDR of the filter is drawn as a bold line shown in Fig. 2.6 (b), and thus it is confirmed that a DR DR_{div} of the filter based on the divide-and-conquer technique is equal to $DR_{filter1} + 40$ [dB] where $DR_{filter1}$ is a DR of the lower path only. A prototype of the filter has dynamic range of 85 dB under 2.5-V supply voltage in Ref. [62].

Another effective approach using the companding technique is to combine with log domain technique, which is called as dynamically adjustable biasing (DAB) technique [25],[26],[60]. A filter based on the DAB technique and its conceptual waveforms are shown in Fig. 2.7 where all MOSFETs are in weak inversion region. In a DAB-based filter gains of a logarithmic compressor and an exponential expander in a log domain filter change dynamically by a control current I_g, which is equal to αI_{in} for a
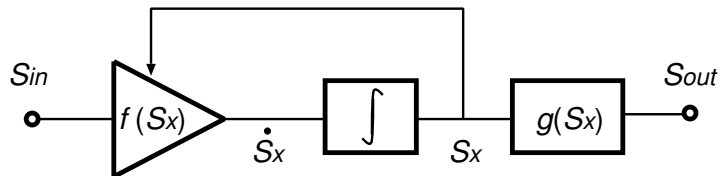
Figure 2.8: Principle of *instantaneous* companding integrator.

coefficient $\alpha > 1$. Since an input voltage V_{ip} of a log domain filter core is expressed as $V_{ip} = nU_T \ln\{(I_{inp} + I_g)/I_b\} + V_b$ where n and U_T are a slope factor and a thermal voltage [2]. A signal swing of the logarithmic compressed voltage, V_{ip}, becomes constant as large as possible as shown in Fig. 2.7. Therefore assuming that a noise from a log domain filter core is dominant, high SNDR is brought for the output over wide input range. The DAB technique is attractive because VGAs in a companding filter shown in Fig. 2.5 are easily implemented by use of only two transistors, M_1 or M_3, and dynamic bias current I_g. Furthermore an SVC circuit is not needed in a DAB-based filter because control current I_g is identified with common-mode input current and canceled out at the output. A prototype filter implemented in a 0.25-μm BiCMOS technology achieves a 112-dB DR at a power supply of 2.5 V [26].

2.3   Companding Technique

A companding circuit is realized by monitoring one or more signals (the input, output, or signals inside the circuit) and changing a gain of the VGAs as shown in Fig. 2.5 [24]. The companding technique is divided into two types according how to monitor the signals. In Fig. 2.5 a control signal has been generated from an envelope of a monitored signal, similarly the divide-and-conquer technique in Fig. 2.6 and DAB technique in Fig. 2.7. As described above, if an envelope of a signal in a companding circuit is used for changing the gain, such circuits are called as *syllabic* companding circuit [24]. On the other hand, an instantaneous signal, not an envelope, might be used as a monitored signal and an example of an integrator are shown in Fig. 2.8, which is called as *instantaneous* companding integrator. In Fig. 2.8 a gain of a com-
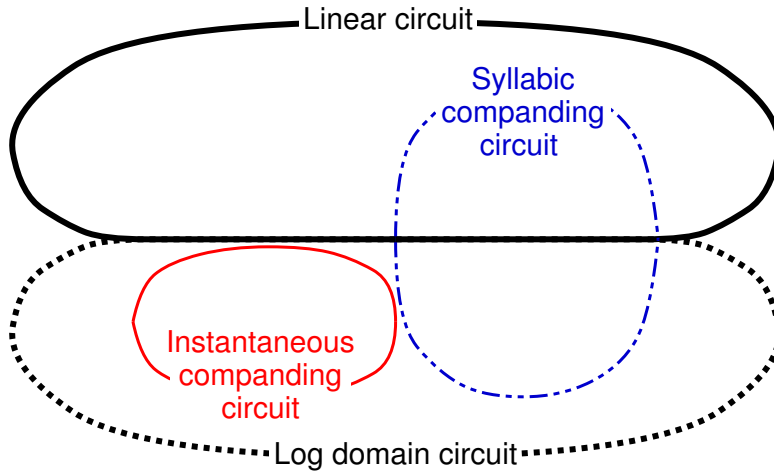
Figure 2.9: Relation among linear circuit, log domain circuit, instantaneous companding circuit, and syllabic companding circuit.

pressor $f(S_x)$ is determined by an instantaneous value of an internal signal S_x, while a gain of an expander $g(S_x)$ is fixed. In an instantaneous companding integrator shown in Fig. 2.8 if a function $g(S_x)$ is arbitrarily given, a required function $f(S_x)$ is specified [24]. An exponential function of a bipolar transistor or a MOSFET is often used as $g(S_x)$ [34], [57], and such circuits are called as instantaneous companding log domain circuit. Therefore a relation among typical linear circuits, log domain circuits, instantaneous companding circuits, and syllabic companding circuits are summarized in Fig. 2.9. In Fig. 2.9 it is assumed that squire-root-domain circuit [49]–[52] is not concerned. Syllabic companding filters the building blocks of which are linear circuit [58], [61], [62] are classified as a region overlapping linear circuit and syllabic companding circuit in Fig. 2.9. On the other hand, DAB-based filters belong to a region overlapping log domain circuit and syllabic companding circuit [25], [26], [60]. Instantaneous and syllabic companding circuits in log domain have a lot of building blocks in common, and thus they are appropriable to each other. The fact helps to simply synthesize higher-order syllabic companding filters [46]. Note that no instantaneous companding circuit using linear building blocks exists because $f(S_x)$ in Fig. 2.8 becomes a constant value $1/K$ for $g(S_x) = KS_x$ with a constant value K, in which a feedback path from S_x to $f(S_x)$ is disconnected [24].

Chapter 3

Synthesis Method of All Low-Voltage CMOS Instantaneous Companding Log Domain Integrators

3.1   Introduction

Instantaneous companding integrators have a lot of design freedom because its configurations are restricted by the only block diagram with non-linear functions [24], [63]. In this chapter a synthesis method of all low-voltage CMOS instantaneous companding log domain integrators is proposed. It is described that required building blocks of CMOS instantaneous companding log domain integrator have variety in terms of their topology and all integrator topologies which include known ones are constructed by combining some building blocks. Known methods [64]–[66] for optimizing parameters, such as device sizes, bias currents and voltages, and so on, can be utilized after a topology is provided or decided. Two 2nd-order Butterworth low-pass filters are fabricated in a 0.35-μm CMOS technology and measured to compare differences of their characteristics. Furthermore some building blocks, which are also applicable to syllabic companding filters, are discussed for easy higher-order filter design.

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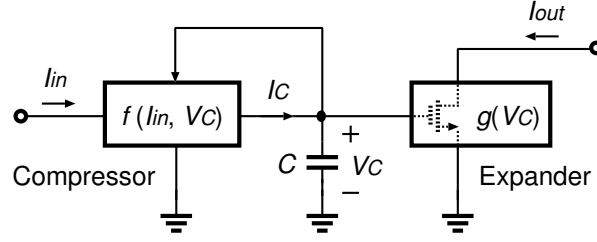
Figure 3.1: CMOS instantaneous companding log domain integrator with a MOSFET in weak inversion region as an expander.

3.2   Principle of CMOS Instantaneous Companding Log Domain Integrator

Figure 3.1 shows a block diagram of instantaneous companding log domain integrators [24]. I_{in}, I_{out}, and blocks f and g are an input and an output currents, a compressor, and an expander, respectively. A compressor f outputs a current I_C flowing into a capacitor C and a voltage V_C of the capacitor is an input of an expander g. In Fig. 2.8,

$$I_{out} = g(V_C) \tag{3.1}$$

and

$$I_C = f(I_{in}, V_C) = C\frac{dV_C}{dt} \tag{3.2}$$

are satisfied. For an integrator with a desired unity-gain angular frequency Ω, I_{in} and I_{out} should relate as

$$\frac{dI_{out}}{dt} = \Omega I_{in}. \tag{3.3}$$

From Eqs. (3.1), (3.2), and (3.3), ΩI_{in} is expressed by

$$\begin{aligned} \Omega I_{in} &= \frac{dI_{out}}{dt} = \frac{dI_{out}}{dV_C}\frac{dV_C}{dt} \\ &= \frac{dg(V_C)}{dV_C}\frac{f(I_{in}, V_C)}{C}. \end{aligned} \tag{3.4}$$

Therefore a compressing function f must satisfy

$$f = I_C = \frac{\Omega C}{\dfrac{dg(V_C)}{dV_C}}I_{in}. \tag{3.5}$$

Assuming that an expander g consists of one n-channel MOSFET in weak inversion region as dashed MOSFET in Fig. 3.1 where its gate-to-source voltage is given by V_C, the function of an expander $g(V_C)$ can be expressed as

$$g = I_{out} = I_S \exp\left(\frac{V_C}{nU_T}\right) \tag{3.6}$$

where I_S is a constant current proportional to an aspect ratio and n and U_T are a slope factor and a thermal voltage, respectively. From Eq. (3.5) the required function of a compressor f can be expressed as

$$f = I_C = \frac{I_B}{I_{out}}I_{in} \tag{3.7}$$

where

$$I_B = nU_T\Omega C. \tag{3.8}$$

Conclusively a CMOS instantaneous companding log domain integrator is obtained by synthesizing a MOSFET in weak inversion region as an expander and a compressor comprised of a current multiplier and divider. Note that a sign of a value of I_B depends on Ω or a type of an integrator: inverting or non-inverting integrator.

3.3   Design Considerations

3.3.1   Expander

A structure of an expander used above is extended. There are two ways to transfer V_C to a gate-to-source voltage of an expander so that Eq. (3.6) still hold. The first one is to drive a gate terminal of the MOSFET through a voltage buffer and a level shifter V_{b1} as shown in Fig. 3.2 (a) where a source potential of an expander should be an arbitrary constant voltage V_{b2}. Another is to do a source terminal through a voltage buffer and a level shifter with a gate potential fixed as in Fig. 3.2 (b). Considering use of a p-channel MOSFET, the other expanders drawn in Figs. 3.2 (c) and (d) are also usable. For all expanders, g is expressed as $g = I_S \exp[(\pm V_C + V_b)/(nU_T)]$ by setting V_{b1} or V_{b2} to an arbitrary constant voltage V_b. From Eq. (3.5) corresponding
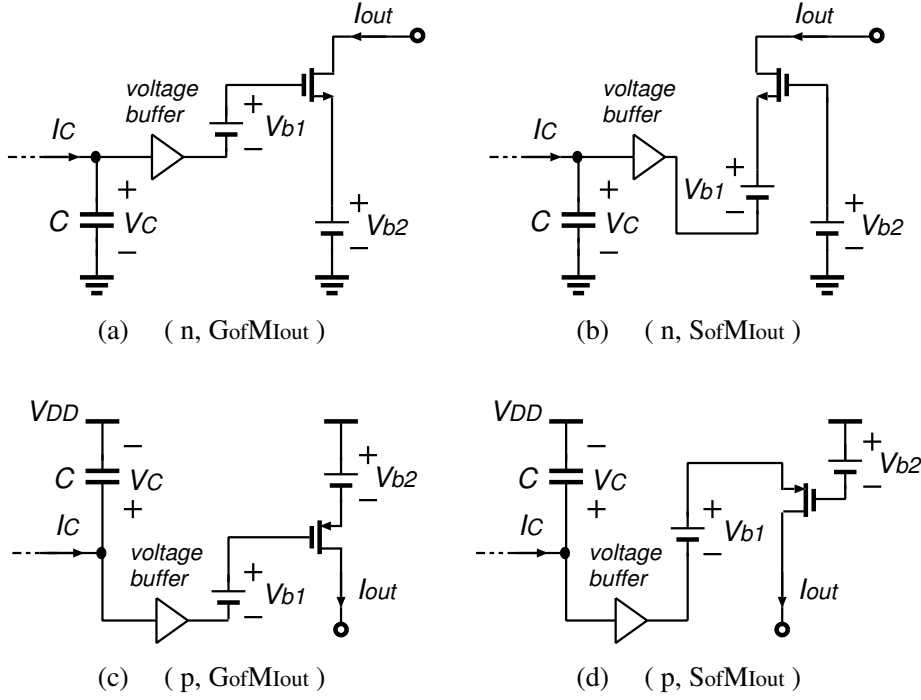
Figure 3.2: All expander configurations expressed as $(TypeM_{exp}, TCV_C)$.

compressing functions become

$$f = I_C = \pm \frac{I_B}{I_{out}} I_{in}. \tag{3.9}$$

The sign of the right-hand side of Eq. (3.9) is positive when a structure of Fig. 3.2 (a) or (d) is used and is negative when that of (b) or (c) is. Any circuit of a family listed in Fig. 3.2 can form part of CMOS instantaneous-companding log domain integrator because Eq. (3.9) is realizable as simple as Eq. (3.7). These four expanding circuits are results of all combinations on the following two freedoms **F1** and **F2**.

F1: Which type of MOSFET is used in an expander; an n-channel or a p-channel MOSFET.

F2: To which terminal of an expanding MOSFET V_C is transmitted; a gate or a source terminal.
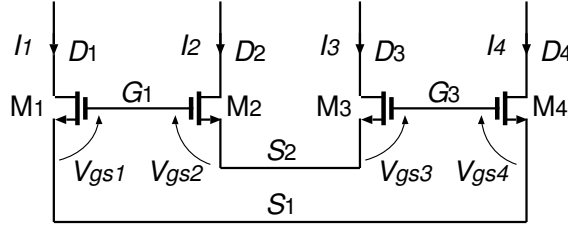
Figure 3.3: Translinear loop (TL).

In order to distinguish design freedoms the following variables are defined. For **F1** a variable $TypeM_{exp}$ is introduced. Its value becomes "n" if an expander is an n-channel MOSFET and it is "p" if that is a p-channel one. As a parameter for **F2** a variable TCV_C is used hereafter. TCV_C equal to "$G_{of}M_{I_{out}}$" if a gate terminal is driven and it does to "$S_{of}M_{I_{out}}$" if a source one is.

3.3.2   Compressor

Current Allocation for Translinear Loop   To implement a current multiplier/divider expressed by Eq. (3.9) which is required as a compressing function, a translinear loop (TL) is used. A TL shown in Fig. 3.3 consists of four n-channel MOSFETs M_1 to M_4 which have the equal aspect ratios. Although a TL consisting of p-channel MOSFETs is also usable of course, it will not be described in the following discussion because the same approach with the followings is available and resulted integrator topologies are mirrored version of those obtained from a TL of n-channel MOSFETs.

Using gate-to-source voltages V_{gsi}'s ($i = 1, 2, 3, 4$) and drain currents I_i's of MOSFETs M_i, $V_{gs1} + V_{gs3} = V_{gs2} + V_{gs4}$ is satisfied and a relation between currents written as

$$I_1 I_3 = I_2 I_4 \tag{3.10}$$

is derived. To realize a function of a compressor in Eq. (3.9), it is considered that I_1,
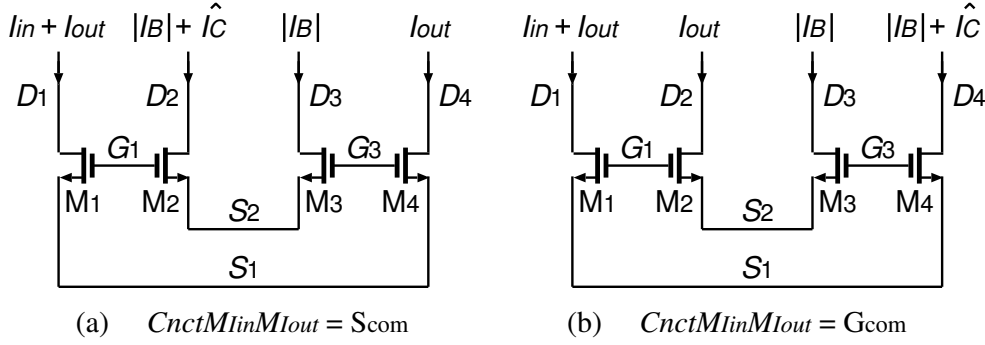
Figure 3.4: Current allocations in a TL for a compressor.

I_2, I_3, and I_4 are set as I_{in}, $\hat{I}_C$, $|I_B|$, and I_{out}, respectively, where

$$\hat{I}_C = \frac{|I_B|I_{in}}{I_{out}} = \pm I_C \, \text{sign}(I_B) \tag{3.11}$$

and $\text{sign}(\cdot)$ is the signum function. I_C which is an alternative current flowing across a capacitor C becomes zero for DC input. Since I_2 must be always positive, let I_2 shifted by a DC current $|I_B|$ [67]. I_1 should be changed to $I_{in} + I_{out}$ to satisfy Eq. .(3.9) by using $I_2 = |I_B| + \hat{I}_C$, $I_3 = |I_B|$, and $I_4 = I_{out}$. Furthermore, Eq. (3.9) is still satisfied even if drain currents of M$_2$ and M$_4$ are interchanged as $I_2 = I_{out}$ and $I_4 = |I_B| + \hat{I}_C$. Eventually two options shown in Fig. 3.4 exist for allocation of drain currents in a TL. Choice from these current assigns is the third freedom on integrator design. As known from Fig. 3.4 this freedom can be described as

F3: Which terminals of two MOSFETs drain current of which are $I_{in} + I_{out}$ and I_{out} are common; gate terminals or source ones.

A variable $CnctM_{I_{in}}M_{I_{out}}$ is employed for **F3**. $CnctM_{I_{in}}M_{I_{out}} = S_{\text{com}}$ corresponds to the use of a TL shown in Fig. 3.4 (a) and $CnctM_{I_{in}}M_{I_{out}} = G_{\text{com}}$ does to that in (b).

Connection of a Capacitor to a TL An output terminal of a compressor is considered. Its output current should be I_C known from Fig. 3.1. Since only $\hat{I}_C$ defined by Eq. (3.11) has relation to I_C in a TL, a capacitor is adjoined to a MOSFET
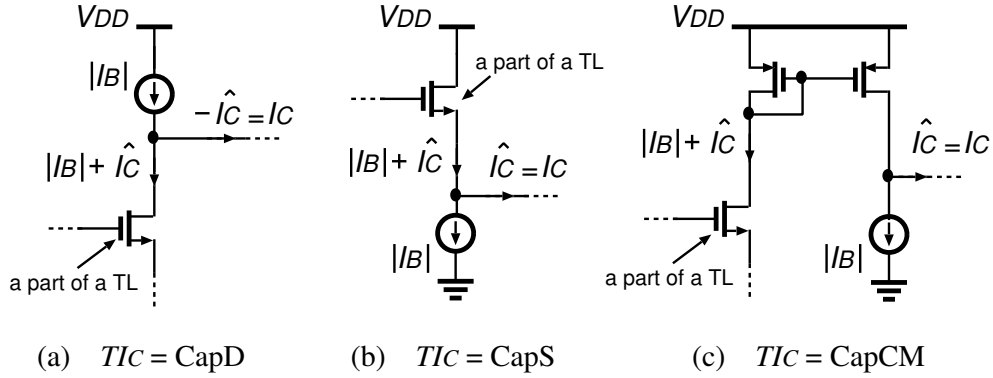
Figure 3.5: Realization of a capacitor current I_C.

with a current $|I_B| + \hat{I}_C$. Three structures shown in Fig. 3.5 can be used. Therefore, the fourth freedom, which has three options, is

F4: How a capacitor C is connected to a MOSFET where $|I_B| + \hat{I}_C$ flows; directly to its drain terminal, to its source one, or to the drain one with a current mirror.

The freedom **F4** introduces a variable TI_C. Its value equals to "CapD" if a capacitor is connected to a drain terminal as shown in Fig. 3.5 (a), to "CapS" if that is done to a source one as in (b), and to "CapCM" if that is done through a p-channel MOSFET current mirror as in (c).

3.3.3   Synthesis Procedures

Topology Design as Combination   All integrators are obtained by use of the four freedoms **F1** to **F4** or as combinations $(TypeM_{exp}, TCV_C, CnctM_{I_{in}}M_{I_{out}}, TI_C)$. For example, a topology proposed in Ref. [36] corresponds to $(TypeM_{exp}, TCV_C, CnctM_{I_{in}}M_{I_{out}}, TI_C) = $ (n, $G_{of}M_{I_{out}}$, S_{com}, CapS) and that in Ref. [41] does to (n, $G_{of}M_{I_{out}}$, S_{com}, CapCM). Thus it is expected that a lot of unknown topologies of integrators are derived from other combinations.

Nevertheless all combinations the total number of which is equal to $2\times2\times2\times3 = 24$ are not realizable. Focusing discussion on a TL, voltages between nodes G_1, G_3, S_1, and S_2 written in Fig. 3.3 must depend on one another because MOSFETs in a TL may not only satisfy Eq. (3.10) but also make a signal path due to synthesis of circuits shown in Figs. 3.2 and 3.5. An n-channel MOSFET corresponding to a drain current $|I_B| + \hat{I}_C$ in Fig. 3.5 may be directly connected to a capacitor and excites a voltage buffer and a level shifter shown in Fig. 3.2 which transfer a voltage signal to a gate or a source terminal of a MOSFET working as an expander. If both of the two MOSFETs in this signal path are included in a TL, two nodal voltages in the TL are related by a level shifter. This synthesis requires a difference of potentials between two nodes of a TL to be fixed although they may independently change with time. Therefore such cases may not be realized. This fact leads designers to a rule that a combination where two MOSFET in a TL have another signal path with a level shifter is discarded. Only one exception to this rule is a case when a gate and a source terminals of M_3 in Fig. 3.4 are connected with a level shifter because of its constant current.

Let prohibited synthesis combination be considered from the above rule. It is only in the case that TI_C=CapS that a gate or a source terminal of MOSFET in a TL becomes an input terminal of a voltage follower and $TypeM_{exp} = $ n is an only case when the level shifter drives another in the same TL. First, $TCV_C = \mathrm{G_{of}M_{I_{out}}}$ is examined. Combinations $(TypeM_{exp}, TCV_C, CnctM_{I_{in}}M_{I_{out}}, TI_C) = $ (n, $\mathrm{G_{of}M_{I_{out}}}$, $\mathrm{S_{com}}$, CapS) and (n, $\mathrm{G_{of}M_{I_{out}}}$, $\mathrm{G_{com}}$, CapS) are illustrated in Fig. 3.6. While the first combination shown in Fig. 3.6 (a) is luckily an exception to the rule, the second one implies a contradiction between a drain current I_1 of M_1 and its gate-to-source voltage. The latter circuit does not operate because this gate-to-source voltage is constant due to a level shifter against a requirement that the voltage varies together with $I_1 = I_{in} + I_{out}$. Thus a prohibited combination is as follows:

PC1: $(TypeM_{exp}, TCV_C, CnctM_{I_{in}}M_{I_{out}}, TI_C) = $ (n, $\mathrm{G_{of}M_{I_{out}}}$,$\mathrm{G_{com}}$, CapS).

Next, another case that $TCV_C = \mathrm{S_{of}M_{I_{out}}}$ is considered. Since a level shifter

(a)   *CnctMIinMIout* = Scom.   (b)   *CnctMIinMIout* = Gcom.
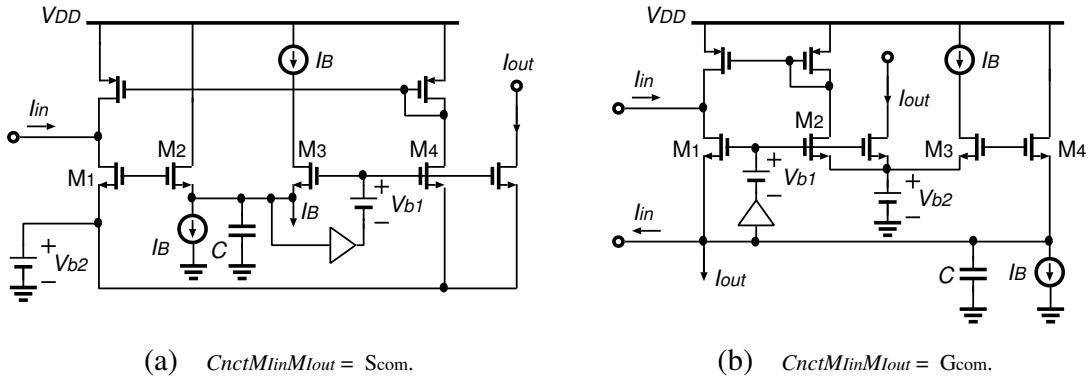
Figure 3.6: Realization of circuits represented as $(TypeM_{exp}, TCV_C, TI_C) = (\text{n},$ $G_{of}M_{I_{out}}, CapS)$.

connects source terminals of two MOSFETs in a TL, $V_{S_1} - V_{S_2}$ is fixed where V_{S_1} and V_{S_2} are nodal voltages of S_1 and S_2 written in Fig. 3.3. However, $V_{S_1} - V_{S_2}$ have to vary with time because $V_{S_1} - V_{S_2}$ can be written by $V_{S_1} - V_{S_2} = nU_T \ln(I_2/I_1) = nUT \ln(I_3/I_4)$ and depends on time-varying input and output signals. Therefore it is concluded that an additional prohibited combination is

PC2: $(TypeM_{exp}, TCV_C, TI_C) = (\text{n}, S_{of}M_{I_{out}}, CapS)$.

Three combinations are removed because of **PC1** and **PC2**. As a consequence, 21 combinations of 24 based on four freedoms **F1** to **F4** are realizable.

Ascertainment of inverting/non-inverting Integrators   The design method described in Sects. 3.1 and 3.2 does not care which type of integrator is obtained from each combination, non-inverting or inverting. Nevertheless a type of each integrator is really deduced from employed values on **F1** to **F4**. The sign of a unity-gain angular frequency Ω is identical with that of I_B as known from Eq. (3.8) and sign(I_B) is determined by Eq. (3.11).

In a case that $TI_C = \text{CapD}$ a relation that $I_C = -\hat{I}_C$ written in Fig. 3.5 leads to sign(I_B) = ∓ 1 where the double sign is used in the same order with Eqs. (3.9) and (3.11) and corresponds to a circuit drawn in Fig. 3.2 (a) or (d) and that in (b) or

(c). On the other hand, if TI_C is equal to CapS or CapCM, $\text{sign}(I_B)$ becomes ± 1. Therefore a sign of a value of Ω $\text{sign}(\Omega) = \text{sign}(I_B)$ and a type of an integrator can be identified; if $(TypeM_{exp}, TCV_C, TI_C)$ is (n, $\text{G}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}$, CapD), (p, $\text{S}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}$, CapD), (n, $\text{S}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}$, CapS), (n, $\text{S}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}$, CapCM), (p, $\text{G}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}$, CapS), or (p, $\text{G}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}$, CapCM), then an inverting integrator is obtained, and otherwise a non-inverting integrator is. This is a result under an assumption that directions of I_{out}'s illustrated in Fig. 3.2 are positive. Here, defining a positive output current as that flowing out of an integrator, the above consideration is summarized as a design step **P1**.

P1: The type of an integrator is ascertained.

The combinations that $(TCV_C, TI_C) = (\text{G}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}$, CapD), $(\text{S}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}$, CapS), and $(\text{S}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}$, CapCM) constitute non-inverting integrators. The other combinations do inverting ones.

Realization of Voltage Buffers and Level shifters A voltage buffer and a level shifter V_{b1} in Fig. 3.2 are implemented with MOSFETs in this section. Generally a voltage buffer may be shorted according to impedance levels of nodes where the buffer and a level shifter are connected. Furthermore a value of V_{b1} may be determined according to the difference voltage level of those nodes. Arbitrariness of a value of V_{b1} can be also utilized for small circuit dimension.

The simplest realization of a voltage buffer and a level shifter is a circuit composed of only a wire shown in Fig. 3.7 (a). This is employed if voltages of input and output terminals of those blocks can be designed to be equal and a ratio of an impedance at a node driving a voltage buffer to a load impedance of a level shifter is much smaller than 1. Table 3.1 summarizes possibility of the 0 level-shift voltage (V_{b1}) and necessity of plus and minus value of V_{b1} for all combinations ($TypeM_{exp}$, TCV_C, $CnctM_{I_{in}}M_{I_{out}}$, TI_C). A "0" means that there is not found a reason why the voltage should be shifted and "+" and "−" do that V_{b1} be positive and negative, respectively. When $(TypeM_{exp}, TCV_C, TI_C) = $ (n, $\text{S}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}$, CapD), a voltage signal of a drain terminal of a MOSFET in a TL is transmitted to a source voltage of another
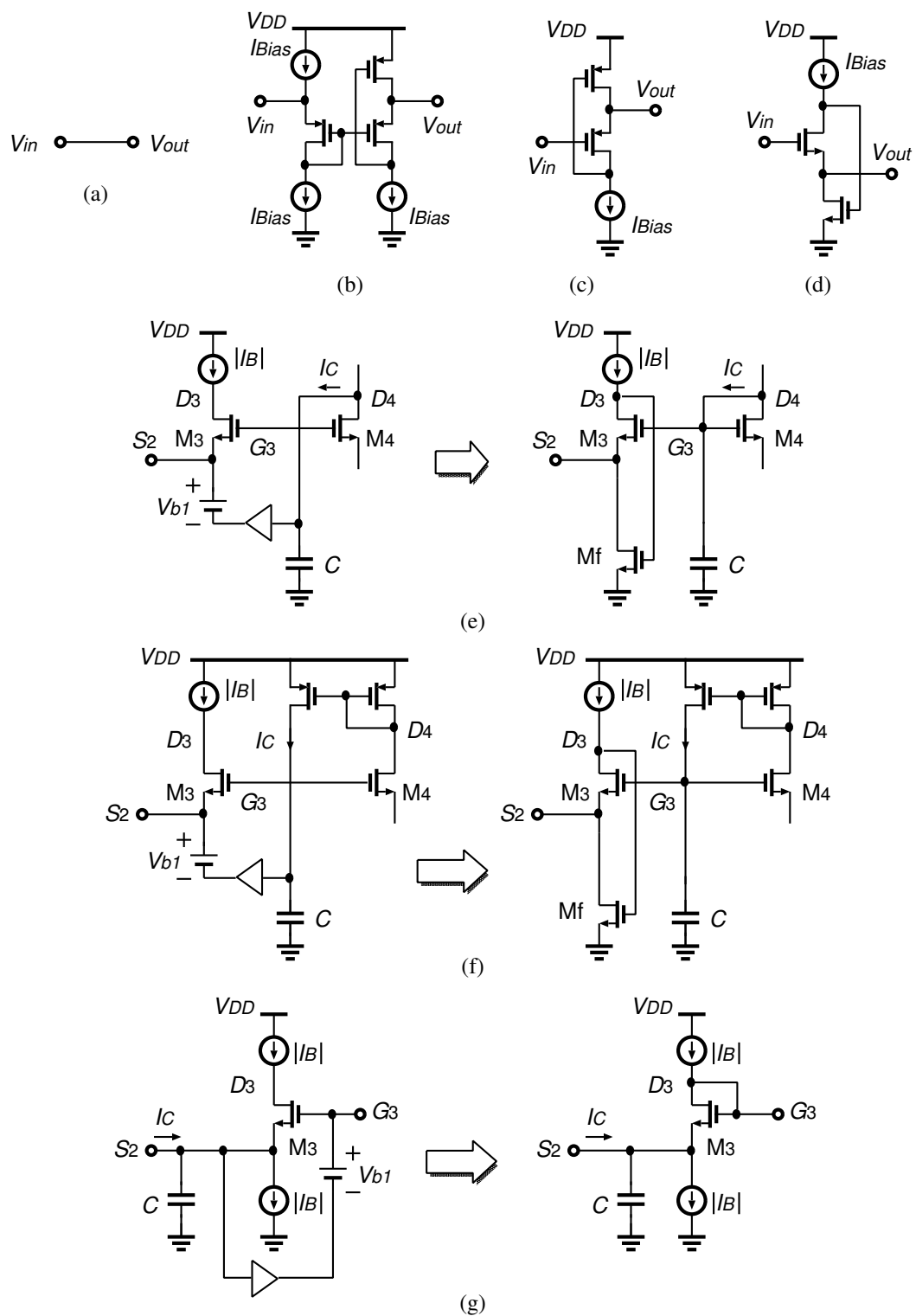
Figure 3.7: Implementation of a voltage buffer and a level shifter.

MOSFET in the same TL. Letting source voltages of all MOSFET in a TL assumed to be similar, a level shifter with $V_{b1} < 0$ is necessary. Another case $(TypeM_{exp},$ $TCV_C, TI_C) = $ (n, $G_{of}M_{I_{out}}$,CapS) is similarly considered although a source voltage is transmitted to a gate one. The third combination requiring $V_{b1} \neq 0$ is $(TypeM_{exp},$ $TCV_C, TI_C) = $ (p, $S_{of}M_{I_{out}}$,CapS). This is because a less than 1.5-V power supply voltage is assumed and is not large enough for a circuit to contain two MOSFETs connected in series of their gate-source voltages. A circuit named as CapCM has a wide output voltage range and is dealt with like one as CapD in the table.

Next, impedance levels relating to input and output terminals of a level shifter are considered. If $TCV_C = G_{of}M_{I_{out}}$, a level shifter excites a gate terminal of a MOSFET and its output impedance does not affect a voltage signal. In Table 3.1, cases where "0" is written and $TCV_C = G_{of}M_{I_{out}}$ are additionally filled with "Fig. 3.7 (a)" expressing that the simplest realization shown in Fig. 3.7 (a) can be used. Other designs to need little shift voltage are replaced by circuit shown in Fig. 3.7 (b). This is composed of a high-input impedance level shifter and a low-output impedance source follower with a shunt feedback structure which is effective for driving a source terminal of an expander. This buffer is appropriate for input and output voltage levels higher than the middle of a supply voltage. Those are denoted as "Fig. 3.7 (b)" in Table 3.1. All combinations designed under $V_{b1} = 0$ are implemented as Figs. 3.7 (a) and (b). On the other hand, positive and negative level shifters shown as "+" and "−", respectively, in Table 3.1 are basically realized by circuits drawn in Figs. 3.7 (c) and (d). The former is used for a design represented as $(TypeM_{exp}, TCV_C, TI_C) =$ (p, $S_{of}M_{I_{out}}$, CapS) and the latter may be for the other design. It is noted that an implementation is simplified together with a MOSFET in a TL as shown in Figs. 3.7 (e) and (f) if $(TypeM_{exp}, CnctM_{I_{in}}M_{I_{out}}, TCV_C, TI_C) =$ (n, $S_{of}M_{I_{out}}$, G_{com}, CapD) and (n, $S_{of}M_{I_{out}}$, G_{com}, CapCM) from the arbitrariness of a value of V_{b1}, respectively. In addition a design of (n, $G_{of}M_{I_{out}}$, G_{com}, CapS) is not available due to **PC1** described in Sect. 3.3.1, and that of (n, $G_{of}M_{I_{out}}$, S_{com}, CapS) requires an exact voltage V_{b1} and should be transformed as in Fig. 3.7 (g).

Table 3.1: Mapping table to replace a voltage buffer and a level shifter.

| | | $(TypeM_{exp}, TCV_C)$ | | | |
		$(n, G_{of}M_{I_{out}})$	$(n, S_{of}M_{I_{out}})$	$(p, G_{of}M_{I_{out}})$	$(p, S_{of}M_{I_{out}})$
TI_C	CapD	0, Fig. 3.7 (a)	—, If $CnctM_{I_{in}}M_{I_{out}} = G_{com}$, then Fig. 3.7 (e) is used. Otherwise Fig. 3.7 (d) is.	0, Fig. 3.7 (a)	0, Fig. 3.7 (b)
	CapS	+, Fig. 3.7 (g) ($CnctM_{I_{in}}M_{I_{out}}$ must be S_{com} due to **PC1**.)	0, Not available according to **PC2**.	0, Fig. 3.7 (a)	+, Fig. 3.7 (c)
	CapCM	0, Fig. 3.7 (a)	—, If $CnctM_{I_{in}}M_{I_{out}} = G_{com}$, then Fig. 3.7 (f) is used. Otherwise Fig. 3.7 (d) is.	0, Fig. 3.7 (a)	0, Fig. 3.7 (b)
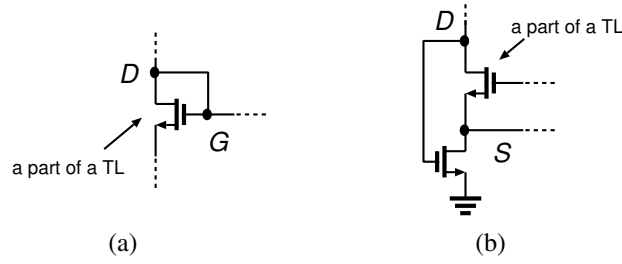
Figure 3.8: Feedback connection to settle a drain voltage.

Eventually the second procedure of an integrator synthesis is as follows:

P2: A voltage buffer and a level shifter are replaced with a circuit shown in Fig. 3.7 referring to Table 3.1.

Procedure for Completion of Integrators There are some nodes voltages of which are not settled yet in each topology based on **F1** to **F4**. Appropriate feedback loops reflecting such voltages of high-impedance nodes must be formed to complete low-voltage CMOS instantaneous companding log domain integrators. Each high-impedance node is a gate terminal or a drain one of a MOSFET in a TL. In addition source terminal nodes S_1 and S_2 in a TL may be also not settled, or current sinking paths from those nodes do not exist. A completion procedure described here contains three design steps: settling all drain voltages of TL's MOSFETs, fixing floating-gate voltages, and resolving problems on S_1 and S_2.

Firstly, it is considered to settle voltages of nodes D_1 to D_4 written in Fig. 3.4 by feedback. For avoiding deterioration of stability, short feedback loops are preferable. Let a voltage of D_i $(i = 1, 2, 3, 4)$ be fed to only a gate terminal or a source one of M_i itself as shown in Fig. 3.8. Thus there exist at most two options of feedback for each D_i. If gate and source terminals have been already in loops to settle their voltages, such terminals should not be in a feedback loop relating to D_i. The number of circuits where all D_i's are fed back is that of combination of those options. Note that any two drain terminals should not be connected to the same terminal S_1, S_2,
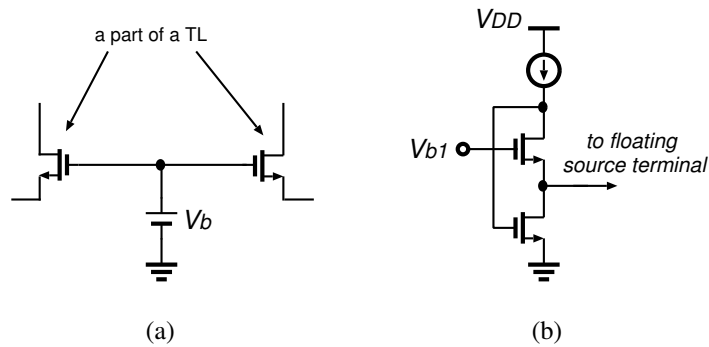
Figure 3.9: Circuits for a floating node.

G_1, or G_3 for guaranteeing drain currents shown in Fig. 3.4.

Next, floating gate terminals in a TL are supplied with DC voltage sources as depicted in Fig. 3.9 (a). Similarly, floating source terminals, which have no current path where drain currents flow out, are driven by a source follower with a low output impedance as shown in Fig. 3.9 (b).

The design described above is summarized by the following procedure:

P3: Completion of connection

(1) Drain terminals of MOSFETs from M_1 to M_4 in a TL are named as D_1 to D_4, respectively.

(2) Tabulate all combinations of terminals to which each D_i is connected where a voltage of D_i is not settled yet. A terminal for D_i to be connected to is a source one S_i or a gate one G_i. A sub-procedure **P3-2** using Table 3.2 described later is called for determining whether D_i has been already in a stable feedback loops or not.

(3) For each combination in $(S_1, S_2, S_3, S_4), \ldots, (G_1, G_2, G_3, G_4)$

(a) if identical terminals are included in the combination under conditions $S_1 = S_4$, $S_2 = S_3$, $G_1 = G_2$, and $G_3 = G_4$, a line " $-$ " are written over those terminals,

and

    (b) if there has already existed a signal loop to settle a voltage of each S_i or G_i, mark " $\times$ " on such a terminal.

(4) For combinations of S_i and G_i without " $\times$ " nor " $-$ " connections shown in Fig. 3.8 (a) and (b) are employed according to G_i and S_i, respectively.

(5) If a gate or a source terminal of a MOSFET in a TL is floating, then a DC voltage source is applied; a voltage reference shown in Fig. 3.9 (a) is for a gate terminal and a low output impedance biasing circuit shown in Fig. 3.9 (b) is for a source terminal.

(6) Resulting connections are distinguished by numbering. A new variable "$CnctN$" taking such numbers will be used.

Next, a method examining whether a terminal of a MOSFET is already settled from only a combination of **F1** to **F4** or not is needed in the second step of the above procedure **P3**. A nodal voltage is stably settled only when a node is connected to a DC voltage source, a capacitor terminal, or a diode-connected MOSFET.

First, MOSFETs connecting to a DC voltage source are considered. Such MOS-FETs are found only in Figs. 3.2 (a) and (b). Their source and gate terminals are driven by DC voltage sources and capacitor nodes. Since a drain current of an expander is fed back through a current mirror circuit, drain terminals of MOSFETs illustrated in Figs. 3.2 (a) and (b) are connected to diode connected MOSFET. Thus, any terminals of an n-channel MOSFET expander do not need additional connection to settle their node voltage. In other words, if $(TypeM_{exp}, CnctM_{I_{in}}M_{I_{out}}) =$ (n, S_{com}), any connection shown in Fig. 3.8 cannot be applied to D_4, G_3, nor S_1 in Fig. 3.4 (a) and those should be overwritten with " $\times$ " in a table made in **P3**. If $(TypeM_{exp}, CnctM_{I_{in}}M_{I_{out}}) =$ (n, G_{com}), then D_2, G_1, and S_2 are excluded from the table. These cases are written as **#1** in Table 3.2 showing nodes voltage of which are settled without additional feedback connection.

Table 3.2: Connected terminals.

$Type M_{exp}$ / Cnct M_{Iin} M_{Iout}	n					p			
	S_{com}		G_{com}			S_{com}		G_{com}	
TI_C	CapD or CapCM	CapS	CapD or CapCM		CapS	CapD or CapCM	CapS	CapD or CapCM	CapS
TCV_C			$S_{of}M_{Iout}$	$G_{of}M_{Iout}$					
#1	D_4, G_3, S_1	D_4, G_3, S_1		D_2, G_1, S_2	D_4, S_1				D_4, S_1
#2	D_2	D_2, S_2		D_4		D_2	D_2, S_2	D_4	
#3			D_3, G_3						
#4		D_3 *1							
Combination group	case A	case B	case C	case D	NA*2	case E	case F	case G	case H

*1 : when $TCV_C = G_{of}M_{Iout}$.

*2 : according to PC1 or PC2.

Second, focusing on a terminal connecting to a capacitor, a MOSFET appearing in Figs. 3.5 (a), (b) and (c) are considered. A drain terminal of a MOSFET with a drain current $|I_B| + \hat{I}_C$ does not need a feedback loop for all cases of TI_C. Use of TI_C=CapS also guarantees that a source terminal of such a MOSFET has been already included in a feedback loop with a large DC loop gain. These are denoted as **#2** in Table 3.2. As written in Fig. 3.5, if $(CnctM_{I_{in}}M_{I_{out}}, TI_C) = (\text{S}_{\text{com}}, \text{CapD})$ or $(\text{S}_{\text{com}}, \text{CapCM})$, D_2 is already connected, and if that is $(\text{G}_{\text{com}}, \text{CapD})$ or $(\text{G}_{\text{com}}, \text{CapCM})$, connection of D_4 is also decided. Furthermore, if $(CnctM_{I_{in}}M_{I_{out}}, TI_C) = (\text{S}_{\text{com}}, \text{CapS})$, it is found that connections of D_2 and S_2 are already completed and if that is $(\text{G}_{\text{com}}, \text{CapS})$, these of D_4 and S_1 are done.

Finally, considering combinations to which exceptional replacements shown in Figs. 3.7 (e), (f) and (g) are applied, more node should be noted. When the replacement in Figs. 3.7 (e) and (f) are applied, which means that $(TypeM_{exp}, TCV_C, CnctM_{I_{in}}M_{I_{out}}, TI_C) = (\text{n}, \text{S}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}, \text{G}_{\text{com}}, \text{CapD})$ and $(\text{n}, \text{S}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}, \text{G}_{\text{com}}, \text{CapCM})$, respectively, a drain terminal D_3 and a gate one G_3 of a MOSFET M_3 are connected to settle their voltage. On the other hand, in the replacement of Fig. 3.7 (g), which is necessary for $(\text{n}, \text{G}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}, \text{S}_{\text{com}}, \text{CapS})$, connections of D_3 is. These special cases are summarized as **#3** and **#4**, respectively, in Table 3.2.

As a consequence, **P3-2** is stated as follows.

P3-2: Table 3.2 is looked up for knowing terminals which are in DC feedback loops by only synthesis of building blocks explained before according to a combination of the freedoms.

3.3.4   An Example and Summary of Proposed Design Procedure

A proposed design procedure is described by use of an example of combinations of the four freedoms **F1** to **F4**. Here a combination of $(TypeM_{exp}, TCV_C, CnctM_{I_{in}}M_{I_{out}}, TI_C) = (\text{p}, \text{G}_{\text{of}}\text{M}_{\text{I}_{\text{out}}}, \text{S}_{\text{com}}, \text{CapD})$, which is composed of building blocks shown in Figs. 3.2 (c), 3.4 (a), and 3.5 (a), is chosen as an example. Thereby a configuration shown in Fig. 3.10 (a) is considered. It is verified that this configuration

(a) Just after executing **P2**.

(b) Resultant circuit numbered as $CnctN = 1$.

(c) Resultant circuit numbered as $CnctN = 2$.

(d) Resultant circuit numbered as $CnctN = 3$.

(e) Resultant circuit numbered as $CnctN = 4$.
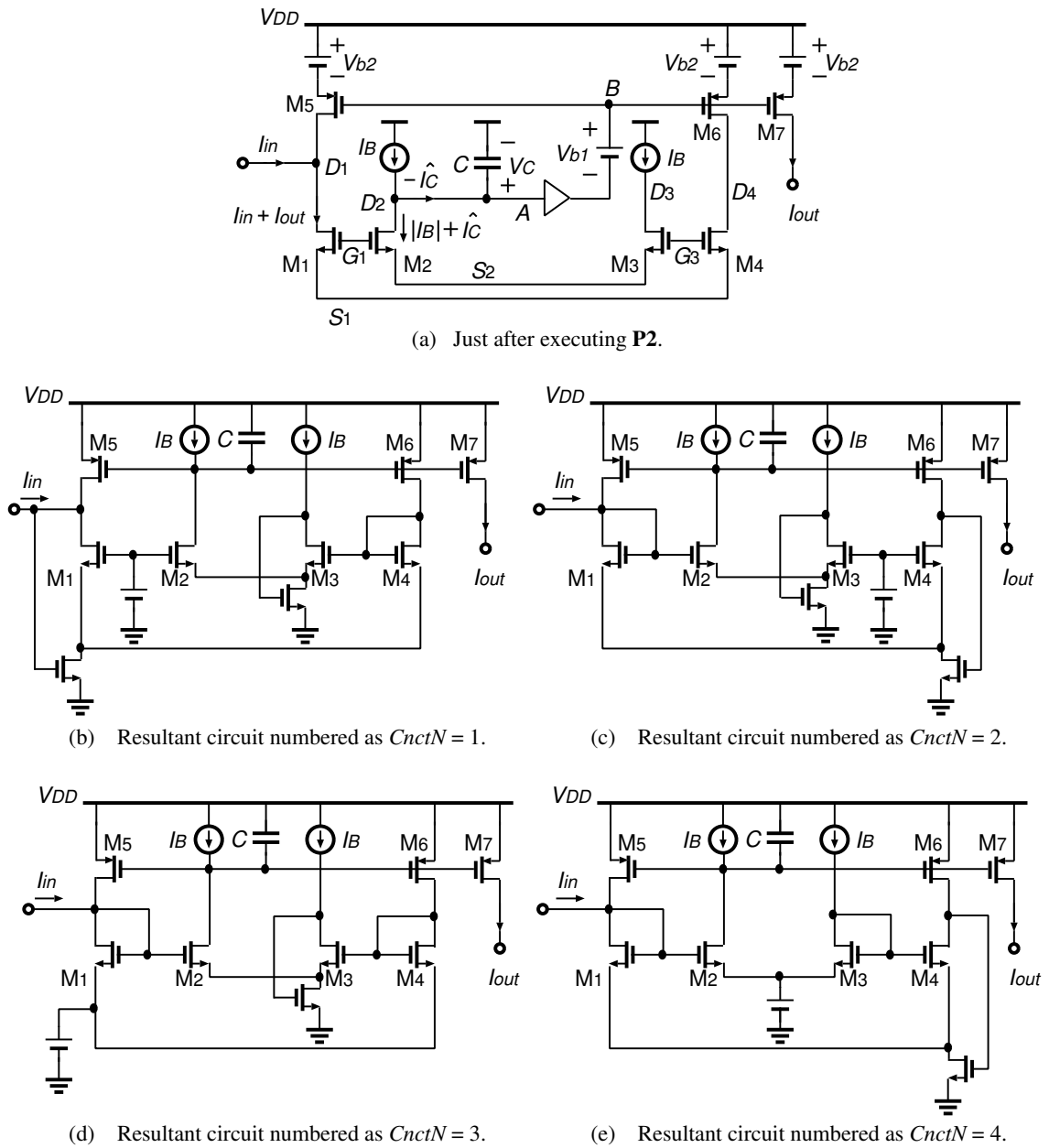
Figure 3.10: Design examples.

is realizable because this combination does not apply to **PC1** nor **PC2**. It is found that this configuration becomes a non-inverting integrator from **P1**. Next, executing **P2**, which is the procedure of the replacement for a voltage buffer and a level shifter, these elements between the nodes A and B in Fig. 3.10 (a) are shorted by using a

Table 3.3: Connections for each drain terminal and prohibited connections in Fig. 3.10 (a).

D_1	D_2	D_3	D_4	Realizable?
S_1	$\times$	S_2	S_1	No (due to $S_1 = S_4$)
S_1	$\times$	S_2	G_3	Yes
S_1	$\times$	G_3	S_1	No (due to $S_1 = S_4$)
S_1	$\times$	G_3	G_3	No (due to $G_3 = G_4$)
G_1	$\times$	S_2	S_1	Yes
G_1	$\times$	S_2	G_3	Yes
G_1	$\times$	G_3	S_1	Yes
G_1	$\times$	G_3	G_3	No (due to $G_3 = G_4$)

wire shown in Fig. 3.7 (a) based on Table 3.1. Finally, following **P3**, connections of some floating terminals are decided. It is known from Table 3.2 that this configuration includes a structure so that a voltage of only D_2 is stably settled, and thus the other terminals D_1, D_3, D_4, G_1, G_3, S_1, and S_2 should be in negative feedback loops or be supplied by DC voltage sources. D_i ($i = 1, 3, 4$) is connected to S_i through a circuit depicted in Fig. 3.8 (b) or to G_i with the diode connection. Terminals where all D_i's are connected are summarized in Table 3.3. There are obviously 8 candidates. Since 4 of them cannot be used from (3) and (4) of **P3**, the others are used as integrators. The resultant circuits are shown in Fig. 3.10 (b) to (e). As known from the above design example corresponding to one combination of the freedom parameters, all topologies of all low-voltage CMOS instantaneous companding log domain integrators are obtained by executing the procedures **P1** to **P3** for all the combinations on **F1** to **F4**.

The proposed synthesis flow is concluded as shown in Fig. 3.11 (a). For each combination of **F1** to **F4**, check with **PC1** and **PC2** is necessary before design on transistor level. If a combination means a realizable topology, **P1** which outputs a result of inverting or non-inverting type of the integrators and **P2** in which the voltage buffers and level shifters are implemented by MOSFETs are executed simultaneously. All connections of MOSFET are decided by **P3** following **P2** and all generated inte-
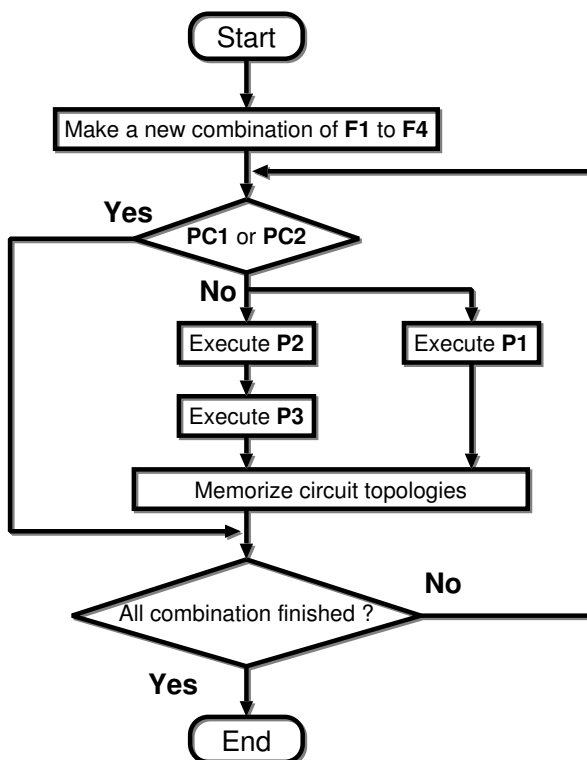
(a) Proposed synthesis flow.
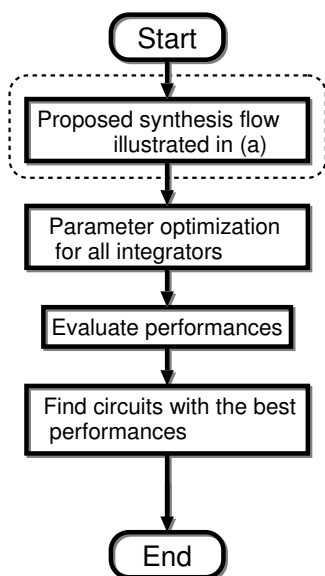
(b) Optimum circuit design.
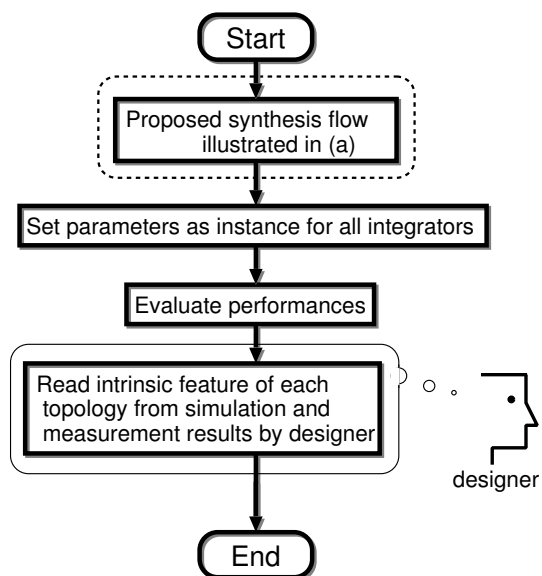
(c) Reading intrinsic features
of each topology.

Figure 3.11: Proposed synthesis flow and its application examples.

grators are memorized.

All tables generated by **P3** are shown in Table 3.4. The obtained integrators are categorized into 8 groups corresponding to **Case A** to **H** of Table 3.2. Each table is written by the same way with Table 3.3. A variable "$CnctN$" is used for distinction of realizable circuit topologies corresponding to each freedom combination. For example, there is only one realizable integrator topology for a combination (n, $G_{of}MI_{out}$, S_{com}, CapD) because the maximum number of $CnctN$ in Table 3.4 (a) is 1. On the other hand 4 topologies have been brought from Table 3.4 (e) for (p, $G_{of}M_{I_{out}}$, S_{com}, CapD). 45 topologies are obtained in total.

Figures 3.11 (b) and (c) show procedures of design of the optimum circuits and finding out new useful knowledges for design, respectively, as application of the proposed synthesis method. In the former example the known methods for optimizing parameter, such as presented in Refs. [64]–[66], can be applied. In the latter it can be known that intrinsic feature of each topology may be also read from characteristic simulation results although some parameter sets to all generated integrators are examined.

Table 3.4: The all connections of each terminals for 21 combinations.

(a) **Case A** in Table 3.2;
D_2, D_4, G_3, and S_1 must be excluded.
(n, $G_{of}M_{I_{out}}$, S_{com}, CapD),
(n, $G_{of}M_{I_{out}}$, S_{com}, CapCM),
(n, $S_{of}M_{I_{out}}$, S_{com}, CapD),
(n, $S_{of}M_{I_{out}}$, S_{com}, CapCM)

D_1	D_2	D_3	D_4	$CnctN$
~~S_1~~	×	S_2	×	—
~~S_1~~	×	~~G_3~~	×	—
G_1	×	S_2	×	1
G_1	×	~~G_3~~	×	—

(b) **Case D** in Table 3.2;
D_2, D_4, G_1, and S_2 must be excluded.
(n, $G_{of}M_{I_{out}}$, G_{com}, CapD),
(n, $G_{of}M_{I_{out}}$, G_{com}, CapCM)

D_1	D_2	D_3	D_4	$CnctN$
S_1	×	~~S_2~~	×	—
S_1	×	G_3	×	1
~~G_1~~	×	~~S_2~~	×	—
~~G_1~~	×	G_3	×	—

(c) **Case B** in Table 3.2;
D_2, D_3, D_4, G_3, S_1 and S_2 must be excluded.
(n, $G_{of}M_{I_{out}}$, S_{com}, CapS)

D_1	D_2	D_3	D_4	$CnctN$
~~S_1~~	×	×	×	—
G_1	×	×	×	1

(d) **Case C** in Table 3.2;
D_2, D_3, D_4, G_1, G_3 and S_2 must be excluded.
(n, $S_{of}M_{I_{out}}$, G_{com}, CapD),
(n, $S_{of}M_{I_{out}}$, G_{com}, CapCM)

D_1	D_2	D_3	D_4	$CnctN$
S_1	×	×	×	1
~~G_1~~	×	×	×	—

(e) **Case E** in Table 3.2;
D_2 must be excluded.
(p, $G_{of}M_{I_{out}}$, S_{com}, CapD),
(p, $G_{of}M_{I_{out}}$, S_{com}, CapCM),
(p, $S_{of}M_{I_{out}}$, S_{com}, CapD),
(p, $S_{of}M_{I_{out}}$, S_{com}, CapCM)

D_1	D_2	D_3	D_4	$CnctN$
~~S_1~~	×	S_2	~~S_1~~	—
S_1	×	S_2	G_3	1
~~S_1~~	×	G_3	~~S_1~~	—
S_1	×	~~G_3~~	~~G_3~~	—
G_1	×	S_2	S_1	2
G_1	×	S_2	G_3	3
G_1	×	G_3	S_1	4
G_1	×	~~G_3~~	~~G_3~~	—

(f) **Case G** in Table 3.2;
D_4 must be excluded.
(p, $G_{of}M_{I_{out}}$, G_{com}, CapD),
(p, $G_{of}M_{I_{out}}$, G_{com}, CapCM),
(p, $S_{of}M_{I_{out}}$, G_{com}, CapD),
(p, $S_{of}M_{I_{out}}$, G_{com}, CapCM)

D_1	D_2	D_3	D_4	$CnctN$
S_1	S_2	~~S_2~~	×	—
S_1	S_2	G_3	×	1
S_1	G_1	S_2	×	2
S_1	G_1	G_3	×	3
G_1	~~S_2~~	~~S_2~~	×	—
G_1	S_2	G_3	×	4
~~G_1~~	~~G_1~~	S_2	×	—
~~G_1~~	~~G_1~~	G_3	×	—

(g) **Case F** in Table 3.2;
D_2 and S_2 must be excluded.
(p, $G_{of}M_{I_{out}}$, S_{com}, CapS),
(p, $S_{of}M_{I_{out}}$, S_{com}, CapS)

D_1	D_2	D_3	D_4	$CnctN$
~~S_1~~	×	~~S_2~~	~~S_1~~	—
S_1	×	~~S_2~~	G_3	—
~~S_1~~	×	G_3	~~S_1~~	—
S_1	×	~~G_3~~	~~G_3~~	—
G_1	×	~~S_2~~	S_1	—
G_1	×	~~S_2~~	G_3	—
G_1	×	G_3	S_1	1
G_1	×	~~G_3~~	~~G_3~~	—

(h) **Case H** in Table 3.2;
D_4 and S_1 must be excluded.
(p, $G_{of}M_{I_{out}}$, G_{com}, CapS),
(p, $S_{of}M_{I_{out}}$, G_{com}, CapS)

D_1	D_2	D_3	D_4	$CnctN$
~~S_1~~	S_2	~~S_2~~	×	—
~~S_1~~	S_2	G_3	×	—
~~S_1~~	G_1	S_2	×	—
~~S_1~~	G_1	G_3	×	—
G_1	~~S_2~~	~~S_2~~	×	—
G_1	S_2	G_3	×	1
~~G_1~~	~~G_1~~	S_2	×	—
~~G_1~~	~~G_1~~	G_3	×	—

3.4   Synthesis Examples

In this section, it is confirmed that all the 45 topologies work as integrators, that is, the feasibility of the proposed design flow shown in Fig. 3.11. Based on the procedure illustrated in Fig. 3.11 (c) some differences resulted from circuit topologies themselves will be also revealed by HSPICE simulation so that knowledges for circuit design are verified.

All integrators are designed to have a 100-kHz unity-gain frequency with a 50-pF capacitor. Let the channel width and length of all n-channel MOSFETs in each integrator be 40 μm and 1 μm, respectively, and those of all p-channel MOSFETs be 80 μm and 1 μm for omitting parameter optimization step in the design flow in this design example. While these setting design parameters limit design space and probably fail to find the optimum circuit in this example, it can be known that all the topologies are functional and intrinsic feature of each topology may be also read from characteristic simulation results. DC gain, consumed current, total harmonic distortion (THD) of an output current for $I_{in} = 1.0\mu\text{A} \times \sin(2\pi \times 100\text{kHz})$, and output current noise over DC to 10 MHz under a 1.0-V supply voltage as an example are simulated by use of parameters of a 0.35-μm CMOS process, and other characteristics than these can be considered if necessary. Since integrators are unstable for a DC input, the 1st-order low-pass filters (LPF's) using the integrators with 100-% negative feedback are simulated here.

Table 3.5 shows characteristics of all integrators. In the table values are simulation results where a DC current $|I_B|$ of each integrator is adjusted to achieve a 100-kHz cutoff frequency. The sensitivity of a DC gain with respect to a supply voltage variation $S_{V_{DD}}^{G_{DC}}$ is computed by

$$S_{V_{DD}}^{G_{DC}} = \frac{\sum_{i=1}^{n} \left(V_{DDi} - \overline{V_{DDi}} \right) \left(G_{DC_i} - \overline{G_{DC}} \right)}{\sum_{i=1}^{n} \left(V_{DDi} - \overline{V_{DD}} \right)^2} \tag{3.12}$$

where V_{DDi} is the i-th sample of supply voltage and $\overline{V_{DD}}$ means a mean value of

Table 3.5: Characteristics of all the generated CMOS log-domain integrators with a 100% negative feedback applied.

$(TypeM_{exp},TCV_C,$ $CnctM_{I_{in}},M_{I_{out}},TI_C,CnctN)$	Type $(+/-)$*1	DC gain	Current consumption	THD*2	$\left\|S^{G_{DC}}_{V_{DD}}\right\|$ *3	Output noise DC–10 MHz	Remark
(n,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapD,1)	+	1.05 dB	10.41 μA	0.77 %	6.09 dB/V	4.11 nA$_{rms}$	—
(n,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapS,1)	−	−1.58 dB	8.62 μA	0.95 %	5.72 dB/V	3.62 nA$_{rms}$	Ref. [36]
(n,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapCM,1)	−	−2.66 dB	11.16 μA	0.38 %	8.73 dB/V	2.91 nA$_{rms}$	Ref. [41]
(n,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,1)	+	1.46 dB	11.41 μA	0.65 %	6.76 dB/V	4.84 nA$_{rms}$	—
(n,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,1)	−	−2.88 dB	11.35 μA	0.52 %	3.29 dB/V	2.82 nA$_{rms}$	—
(n,S$_{of}$M$_{I_{out}}$,S$_{com}$,CapD,1)	−	−1.32 dB	8.17 μA	0.51 %	3.94 dB/V	3.07 nA$_{rms}$	—
(n,S$_{of}$M$_{I_{out}}$,S$_{com}$,CapCM,1)	+	0.78 dB	15.57 μA	1.21 %	9.47 dB/V	3.86 nA$_{rms}$	—
(n,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,1)	−	−2.19 dB	6.46 μA	1.06 %	3.54 dB/V	3.03 nA$_{rms}$	Ref. [32]
(n,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,1)	+	3.58 dB	16.50 μA	0.33 %	14.65 dB/V	4.96 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapD,1)	+	−1.94 dB	8.96 μA	0.45 %	4.37 dB/V	3.77 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapD,2)	+	−0.69 dB	9.43 μA	0.28 %	5.25 dB/V	3.73 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapD,3)	+	−1.36 dB	10.89 μA	0.17 %	4.97 dB/V	3.69 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapD,4)	+	−0.37 dB	11.02 μA	0.19 %	5.30 dB/V	3.71 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapS,1)	−	0.57 dB	17.11 μA	1.26 %	5.85 dB/V	5.01 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapCM,1)	−	0.26 dB	15.53 μA	0.79 %	1.90 dB/V	4.39 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapCM,2)	−	0.36 dB	15.92 μA	0.74 %	1.35 dB/V	4.40 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapCM,3)	−	0.31 dB	16.93 μA	0.75 %	0.27 dB/V	4.38 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,S$_{com}$,CapCM,4)	−	0.76 dB	18.12 μA	0.71 %	0.95 dB/V	4.41 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,1)	+	−0.86 dB	9.55 μA	0.28 %	4.79 dB/V	3.87 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,2)	+	−1.77 dB	9.08 μA	0.62 %	4.34 dB/V	3.85 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,3)	+	−1.32 dB	10.42 μA	0.41 %	4.63 dB/V	3.84 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,4)	+	−0.75 dB	10.86 μA	0.26 %	5.26 dB/V	3.72 nA$_{rms}$	Ref. [67]

*1 "+": non-inverting, "−": inverting integrator.

*2 $I_{in} = 1.0\mu A \times \sin(2\pi \times 100\text{kHz})$ at $V_{DD} = 1.0$ V.

*3 Sensitivity of the DC gain for the supply voltage V_{DD} given by Eq. (3.12).

Table 3.5: Characteristics of all the generated CMOS log-domain integrators with a 100% negative feedback applied. (continued)

$(TypeM_{exp},TCV_G,$ $CnctM_{I_{in}},M_{I_{out}},TI_C,CnctN)$	Type $(+/-)$ *1	DC gain	Current consumption	THD *2	$\left\|S^{G_{DC}}_{V_{DD}}\right\|$ *3	Output noise DC−10 MHz	Remark Largest THD
(p,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapS,1)	−	0.48 dB	16.01 μA	2.93 %	3.29 dB/V	4.35 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,1)	−	0.41 dB	15.79 μA	0.84 %	0.16 dB/V	4.39 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,2)	−	0 dB	14.94 μA	0.53 %	0.18 dB/V	4.31 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,3)	−	0.23 dB	16.95 μA	0.64 %	0.45 dB/V	4.32 nA$_{rms}$	—
(p,G$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,4)	−	1.18 dB	18.99 μA	0.77 %	1.26 dB/V	4.59 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,1)	−	−2.83 dB	13.68 μA	0.76 %	0.56 dB/V	4.98 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,2)	−	−2.06 dB	13.19 μA	0.24 %	0.79 dB/V	5.28 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,3)	−	−2.42 dB	14.01 μA	0.31 %	0.68 dB/V	5.16 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,4)	−	−1.63 dB	15.18 μA	0.24 %	0.75 dB/V	5.41 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapS,1)	+	−1.16 dB	10.41 μA	0.81 %	1.94 dB/V	3.50 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,1)	+	−2.6 dB	12.99 μA	0.33 %	4.04 dB/V	4.04 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,2)	+	−3.35 dB	12.42 μA	0.49 %	5.41 dB/V	3.86 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,3)	+	−2.91 dB	14.04 μA	0.32 %	5.49 dB/V	3.93 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,4)	+	−3.83 dB	13.67 μA	0.64 %	5.54 dB/V	3.80 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,1)	−	−2.09 dB	13.19 μA	0.16 %	0.66 dB/V	5.23 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,2)	−	−2.59 dB	12.46 μA	0.45 %	0.72 dB/V	5.08 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,3)	−	−2.36 dB	14.19 μA	0.35 %	0.65 dB/V	5.15 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapD,4)	−	−1.6 dB	14.90 μA	0.50 %	0.69 dB/V	5.44 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapS,1)	+	0.6 dB	11.22 μA	0.95 %	0.64 dB/V	3.64 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,1)	+	−3.37 dB	12.57 μA	0.54 %	5.33 dB/V	3.89 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,2)	+	−2.77 dB	12.72 μA	0.35 %	5.05 dB/V	4.01 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,3)	+	−3.05 dB	14.01 μA	0.39 %	5.29 dB/V	3.95 nA$_{rms}$	—
(p,S$_{of}$M$_{I_{out}}$,G$_{com}$,CapCM,4)	+	−3.95 dB	14.12 μA	0.47 %	5.80 dB/V	3.80 nA$_{rms}$	—

*1 "+": non-inverting, "−": inverting integrator.

*2 $I_{in} = 1.0\mu A \times \sin(2\pi \times 100\text{kHz})$ at $V_{DD} = 1.0$ V.

*3 Sensitivity of the DC gain for the supply voltage V_{DD} given by Eq. (3.12).
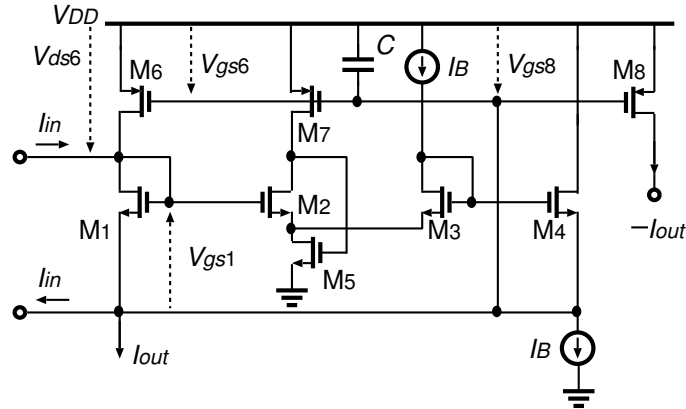
Figure 3.12: Circuit expressed by (p, $G_{of}M_{I_{out}}$, G_{com}, CapS, 1).

V_{DD}'s. G_{DCi} and $\overline{G_{DC}}$ are a DC gain corresponding to V_{DDi} and a DC gain mean value, respectively. $S_{V_{DD}}^{G_{DC}}$ means a slope of the regression line of DC gains and supply voltages. In this simulation, $S_{V_{DD}}^{G_{DC}}$ is obtained by sweeping V_{DD} from 0.8 V to 1.2 V with 41 samples.

In Table 3.5 an integrator noted by a combination (p, $G_{of}M_{I_{out}}$, G_{com}, CapS, 1) has the largest THD in all integrators. This circuit is drawn in Fig. 3.12. A drain-to-source voltage $|V_{ds6}|$ of M_6 is less than 0.1 V because $V_{ds6} = V_{gs8} + V_{gs1} = V_{gs6} + V_{gs1}$ where $V_{gs8} = V_{gs6} \approx -0.6$ and $V_{gs1} \approx 0.55$. This is the reason why the non-linearity of integrator increases. As another characteristic it appears on the whole that the output current noise of an integrator including "n" as $TypeM_{exp}$ tends to be better than that including "p." This better noise performance is attributed to a fewer number of used MOSFETs compared with integrators including "p." Moreover, the integrators including (p, $G_{of}M_{I_{out}}$, CapCM) and (p, $S_{of}M_{I_{out}}$, CapD) have better sensitivity than the others. The reason why there are large differences in sensitivities is not easily identified.
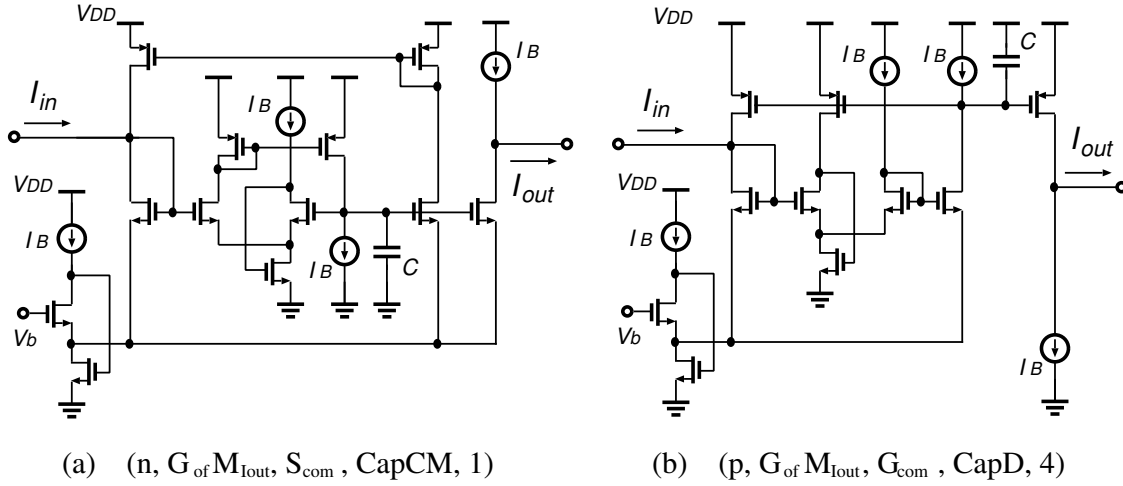
Figure 3.13: Two integrators for 2nd-order Butterworth low-pass filters.
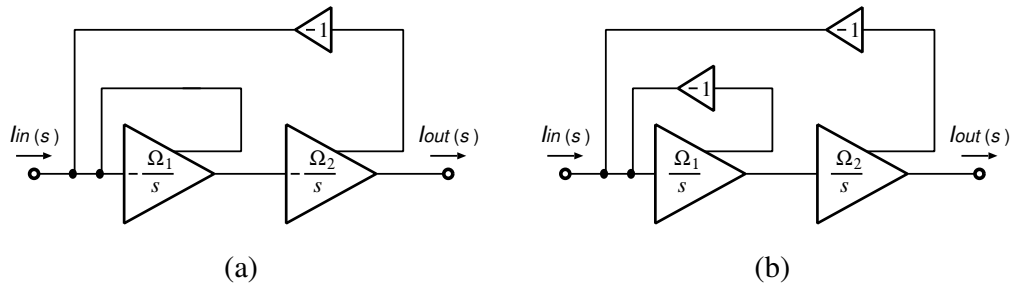
Figure 3.14: 2nd-order low-pass filter structures: (a) for (n, $G_{of}M_{I_{out}}$, S_{com}, CapCM, 1) and (b) for (p, $G_{of}M_{I_{out}}$, G_{com}, CapD, 4).

3.5   Measured Results

Two 2nd-order low-pass filters are designed by using two integrators, (n, $G_{of}M_{I_{out}}$, S_{com}, CapCM, 1) and (p, $G_{of}M_{I_{out}}$, G_{com}, CapD, 4), shown in Fig. 3.13. Since an integrator labeled as (n, $G_{of}M_{I_{out}}$, S_{com}, CapCM, 1) is an inverting type, a 2nd-order biquad structure shown in Fig. 3.14 (a) is employed. On the other hand, a structure shown in Fig. 3.14 (b) is used for (p, $G_{of}M_{I_{out}}$, G_{com}, CapD, 4) because an integrator shown in Fig. 3.13 (b) is a non-inverting type as seen from Table 3.5. The overall 2nd-order low-pass filters are shown in Fig. 3.15. For Butterworth filter characteristic the
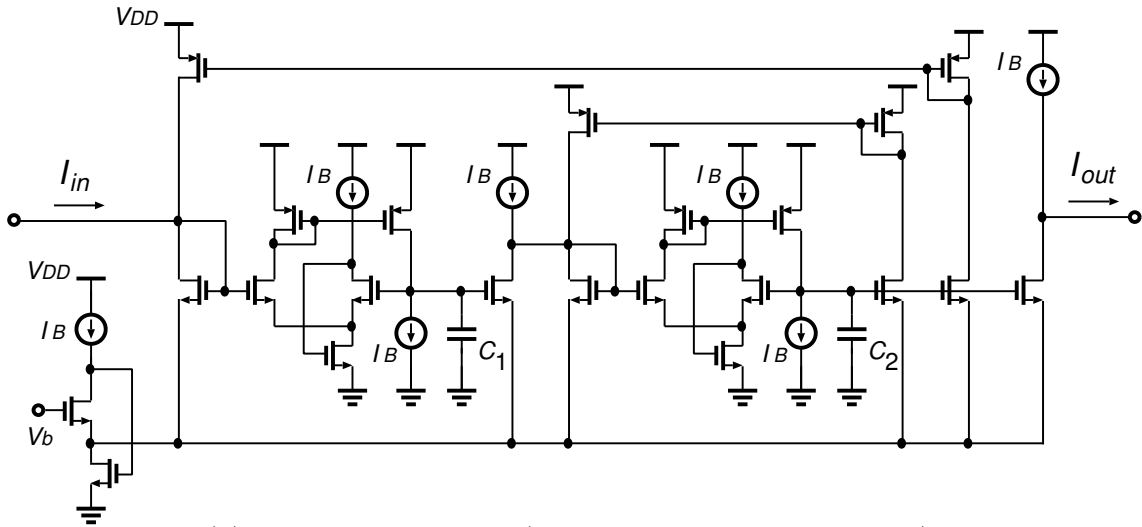
(a) Filter composed of (n, $G_{of}M_{I_{out}}$, S_{com}, CapCM, 1).
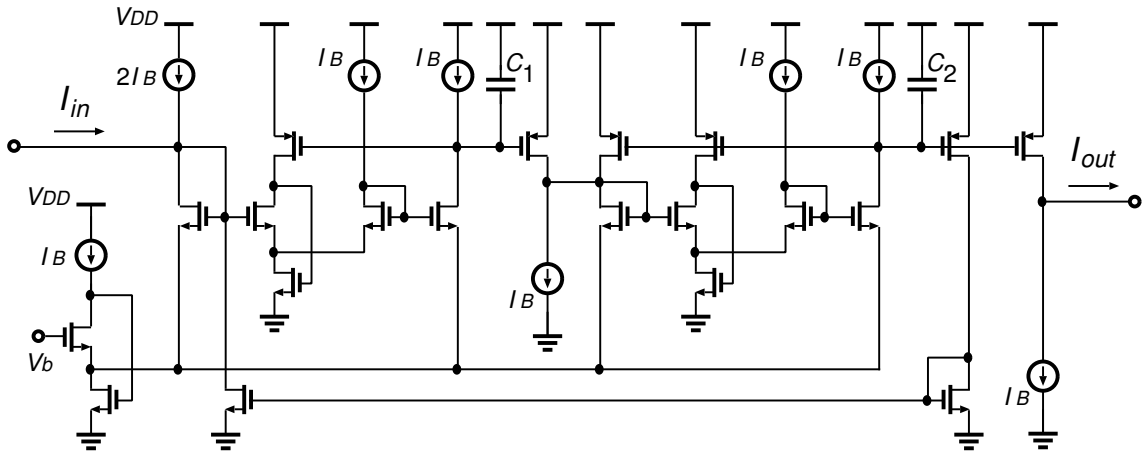
(b) Filter composed of (p, $G_{of}M_{I_{out}}$, G_{com}, CapD, 4).

Figure 3.15: 2nd-order Butterworth low-pass filters.

unity gain angular frequency $\Omega_i = I_B/(nU_TC_i)$ $(i = 1, 2)$ from Eq. (3.8) is expressed as $\Omega_1 = \sqrt{2}\omega_c$ and $\Omega_2 = \omega_c/\sqrt{2}$ where ω_c is equal to a cutoff angular frequency of the filters. Therefore capacitors C_1, C_2, and a bias current I_B are set as 25 pF, 50 pF, and 1 μA, respectively, for 100-kHz cutoff frequency. The filters are fabricated in a 0.35-μm CMOS technology and the microphotographs of the filters are shown in Fig. 3.16.

Figure 3.17 shows measured frequency responses with ideal one. The cutoff frequencies of two filters are 82.3 and 104 kHz, respectively, and their gradient at a
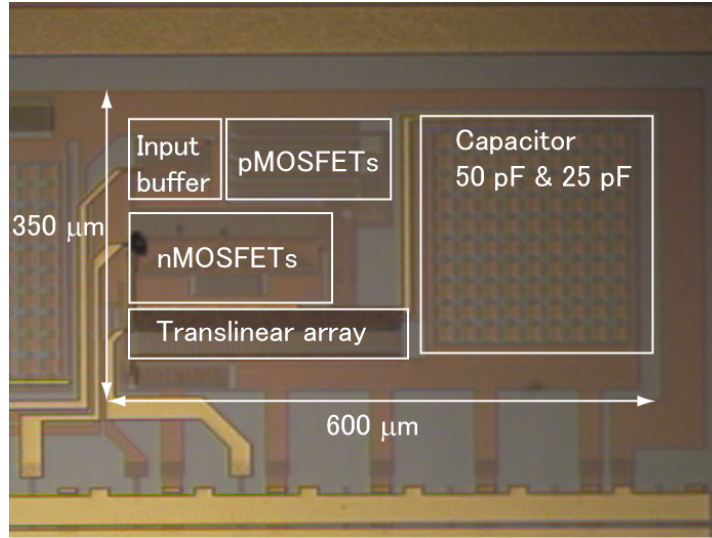
(a) Filter composed of (n, $G_{of}M_{I_{out}}$, S_{com}, CapCM, 1).
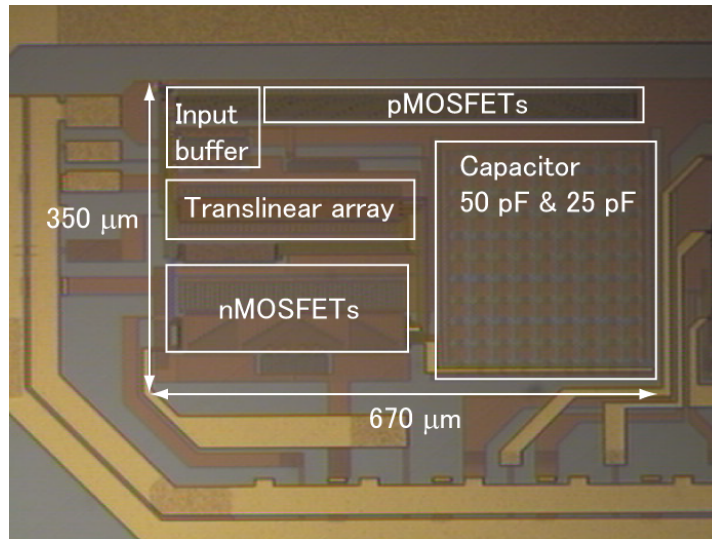
(b) Filter composed of (p, $G_{of}M_{I_{out}}$, G_{com}, CapD, 4).

Figure 3.16: Chip microphotographs of 2nd-order Butterworth low-pass filters.

role off is -40 dB/dec., which is 2nd-order low-pass filter characteristic. Figure 3.18 shows a sensitivity of DC gain for a variation in a power supply voltage V_{DD} which changes from 0.8 V to 1.2 V. In Fig. 3.18 it is confirmed that a filter composed of (p, $G_{of}M_{I_{out}}$, G_{com}, CapD, 4) has lower sensitivity than that of (n, $G_{of}M_{I_{out}}$, S_{com}, CapCM, 1), which is also seen from Table 3.5. Summary of measured characteristics of two filters is shown in Table 3.6. The sensitivity $S_{V_{DD}}^{G_{DC}}$ is calculated by Eq. (3.12).

Measured (n,GofMIout, Scom, CapCM, 1) : ———
Measured (p,GofMIout, Gcom, CapD, 4) : -------
Ideal : - - -
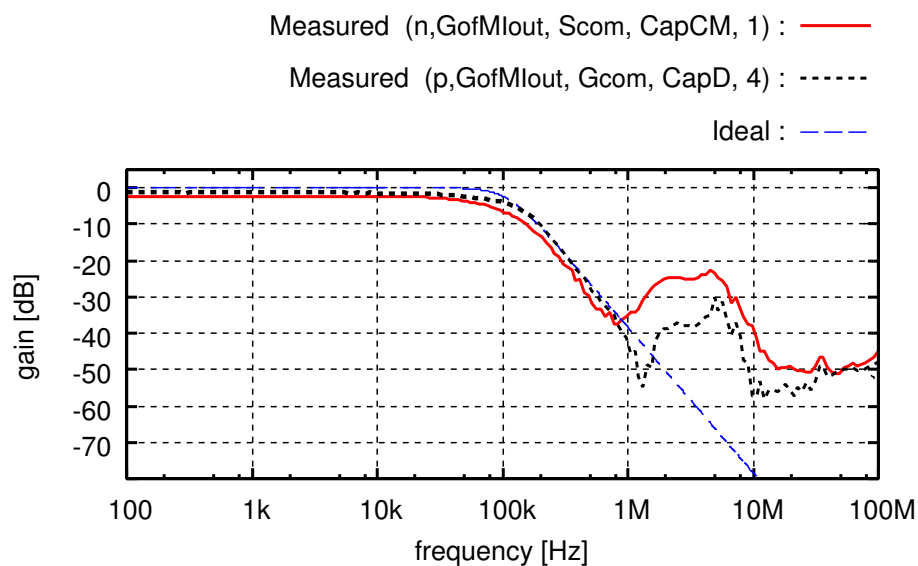
Figure 3.17: Frequency characteristics.

Measured (n,GofMIout, Scom, CapCM, 1) : ◯
Simulated (n,GofMIout, Scom, CapCM, 1) : ———
Measured (p,GofMIout, Gcom, CapD, 4) : △
Simulated (p,GofMIout, Gcom, CapD, 4) : - - -
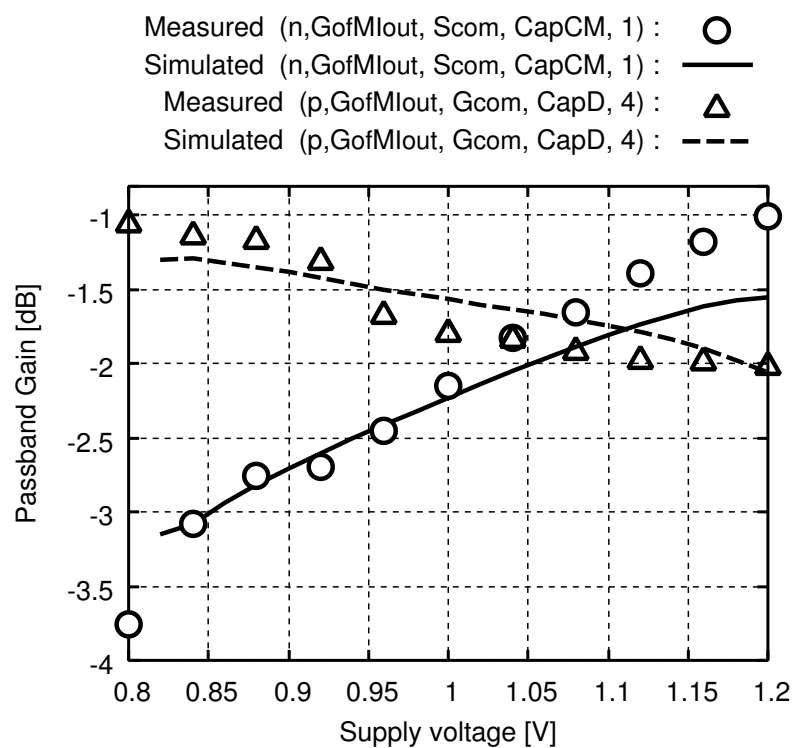
Figure 3.18: Sensitivity of DC gain for variation in a power supply voltage.

Table 3.6: Summary of measured filter characteristics.

	Filter composed of (n, $G_{of}M_{I_{out}}$, S_{com}, CapCM, 1)	Filter composed of (p, $G_{of}M_{I_{out}}$, G_{com}, CapD, 4)
Power supply voltage	1.0 V	1.0 V
Passband gain	−2.29 dB	−1.63 dB
Cutoff freq. (f_{-3dB})	82.3 kHz	104.0 kHz
$\left|S_{V_{DD}}^{G_{DC}}\right|$	4.98 dB/V	2.06 dB/V
Stopband attenuation	−25 dB	−30 dB
Output noise @ DC to cutoff freq.	0.76 nA$_{rms}$	1.07 nA$_{rms}$
THD @ I_{in} : 1.4μA$_{pp}$ 10 kHz	0.73 %	0.98 %
Dynamic range @ THD : −40 dB	54.6 dB	52.4 dB
Active area	0.35×0.6 mm^2	0.35×0.67 mm^2

3.6 Consideration of Log Domain Integrators for Higher-Order Log Domain Filter Synthesis

For higher-order filter design the generated 45 integrators can be used by directly cascading each other as like the prototype filters in the previous section. However if only log domain integrator core, which is a part of an instantaneous companding log domain integrator, is employed for higher-order filter design, then it is possible to simply synthesize a filter.

Principle of instantaneous companding log domain integrator shown in Fig. 3.1 can be redrawn as a block diagram in Fig. 3.19, where a compressor is decomposed to a logarithmic (Log.) compressor and a log domain integrator core. In Fig. 3.19 if the log domain integrator core is replaced with a log domain filter core, which is composed of some integrator cores, then a higher-order filter is simply obtained because of no overlaps of a Log compressor and an exponential (Exp.) expander. Therefore log domain integrator cores are chosen here from the generated 45 integrators in the view of simplicity of higher-order log domain filter core synthesis. Note that potentials of an input and an output voltage in an integrator core must be the same because the core is directly cascaded to others: only topologies with ($TypeM_{exp}$) = n are
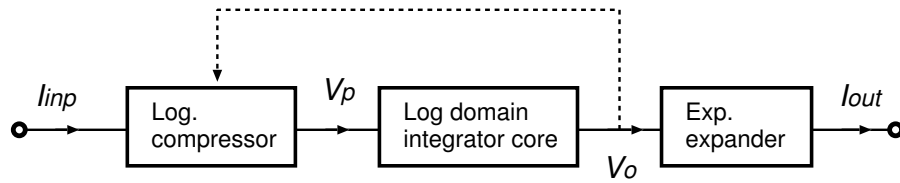
Figure 3.19: Redrawn block diagram of instantaneous companding log domain integrator from Fig. 3.1.
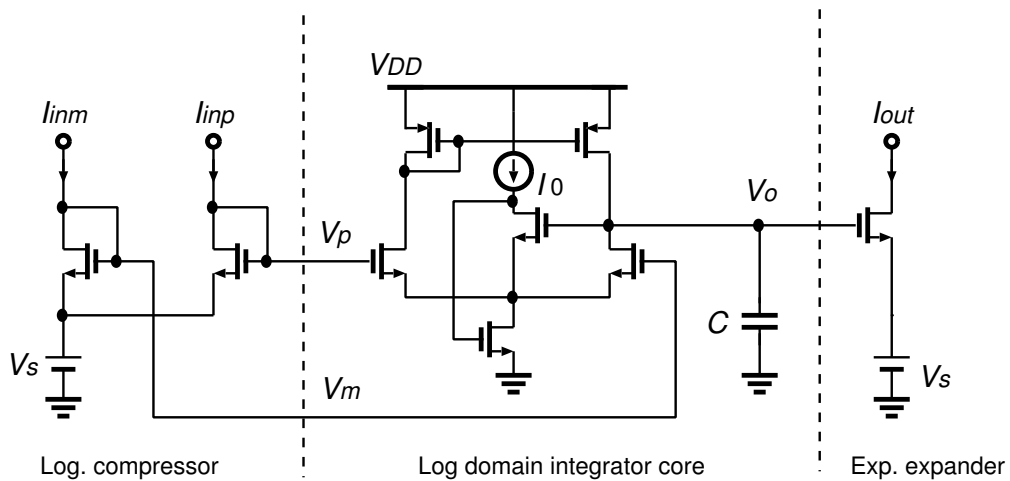
Figure 3.20: Differential input log domain integrator from (n, $G_{of}M_{I_{out}}$, S_{com}, CapD, 1) and (n, $G_{of}M_{I_{out}}$, S_{com}, CapCM, 1).

acceptable. Furthermore a differential input configuration is needed for the cores. From (n, $G_{of}M_{I_{out}}$, S_{com}, CapD, 1) and (n, $G_{of}M_{I_{out}}$, S_{com}, CapCM, 1) a log domain integrator with differential input shown in Fig. 3.20 is obtained. Similarly (n, $S_{of}M_{I_{out}}$, G_{com}, CapD, 1) and (n, $S_{of}M_{I_{out}}$, G_{com}, CapCM, 1) lead to a configuration shown in Fig. 2.2 [33]. The integrators include a log domain integrator core and then a higher-order log domain filter core can be synthesized by use of these integrator cores. Especially, if the syllabic companding technique is applied to the integrator shown in Fig. 3.20, a low-voltage operation can be easily achieve due to its configuration. A details of the log domain filter core synthesis method is described in Appendix A.

3.7 Conclusion

A synthesis method of all low-voltage CMOS instantaneous-companding log domain integrators using design freedoms has been proposed. Forty-five integrators involving four known circuitries are obtained. Simulation results of all the integrators showed different characteristics and comparison of these can find out an integrator satisfying required performance. As an example, two 2nd-order Butterworth low-pass filters are fabricated in a 0.35-μm CMOS technology and its measure results are compared. Furthermore a topology of a log domain integrator core is discussed for higher-order filter design.

Chapter 4

CMOS Syllabic Companding Log Domain Filter for Low-Voltage Operation

4.1   Introduction

The syllabic-companding technique is suitable for realizing wide dynamic range signal processor [23], [24]. Voltage swings of internal nodes in a syllabic companding circuit are almost constant and constant signal-to-noise ratio (SNR) is brought over wide input range. Especially, the dynamically adjustable biasing (DAB) technique, which is combination of the syllabic companding and the log domain techniques [33], [35], [39], is attractive because amplifiers on a DAB-based circuit are easily implemented by use of only one transistor [25], [26]. In this chapter, a modified DAB technique for low-voltage filters is proposed. A nodal voltage which has been fixed in the conventional DAB-based filter is appropriately changed in a proposed one. Two state variable correction (SVC) methods, which are needed to keep an externally linear and time invariant (ELTI) relation between an input and an output, are also proposed for low voltage operation. Simulated results show that the proposed DAB-based filters achieve wide dynamic range under a low-supply voltage and have an ELTI relation due to proposed SVC methods.
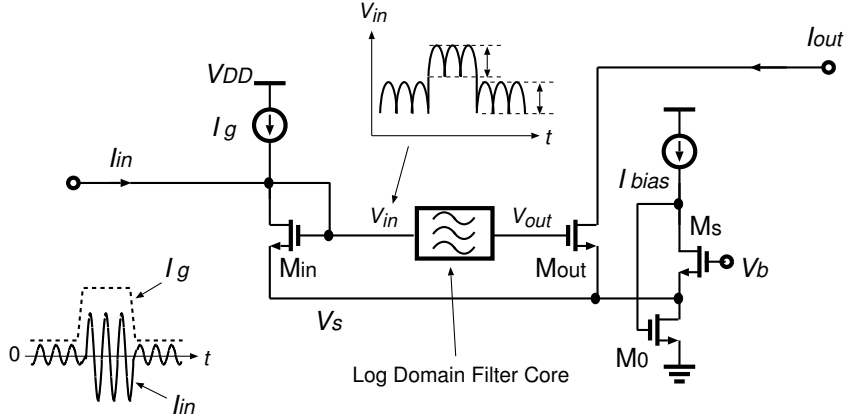
Figure 4.1: Example circuitry of dynamically adjustable biasing (DAB) log domain filters.

4.2   Proposed Low-Voltage Syllabic Companding Integrator in Log Domain

4.2.1   Dynamically Adjustable Biasing Technique

Figure 4.1 shows the DAB-based filter and conceptual waveforms [25], [26]. It is assumed that all MOSFETs are in weak inversion region. A drain current I_d of a MOSFET is a function of its gate-to-source voltage V_{gs} expressed as

$$I_d = I_S \exp\left(\frac{V_{gs}}{nU_T}\right) \tag{4.1}$$

where I_S is a current dependent on a fabrication process and proportional to an aspect ratio, and n and U_T are a slope factor and a thermal voltage, respectively. The diode-connected MOSFET M_{in} in Fig. 4.1 logarithmically converts an input current I_{in} into a voltage V_{in} which is an input voltage of a log domain filter core as a main signal processor. Kirchhoff's voltage law (KVL) gives $V_{in} - nU_T \ln\{(I_{in} + I_g)/I_S\} = V_b - nU_T \ln\{I_{bias}/I_S\}$, and therefore,

$$V_{in} = nU_T \ln\left(\frac{I_{in} + I_g}{I_{bias}}\right) + V_b. \tag{4.2}$$

The MOSFET M$_{\text{out}}$ expands V_{out} to an output current I_{out} with an exponential function as

$$I_{out} = I_{bias} \exp \left(\frac{V_{out} - V_b}{nU_T} \right) \tag{4.3}$$

which is obtained by resolving $V_b - nU_T \ln\{I_{bias}/I_S\} = V_{out} - nU_T \ln\{I_{out}/I_S\}$ from KVL. A control current I_g should be appropriately changed depending on an amplitude of an input current I_{in}. Let I_{in} be factorized in the time domain as $I_{in} = I_{env}(t) \cos[\theta(t)]$ where $I_{env}(t)$ slowly changes at almost time or is an envelope of I_{in} and $\theta(t)$ represents a phase of a higher-frequency signal component with a constant amplitude. Since $I_{env}(t)$ approximates to a constant current in short time, a swing of V_{in} can be given by

$$V_{in}\Big|_{I_{in}=I_{env}} - V_{in}\Big|_{I_{in}=-I_{env}} = nU_T \ln \frac{I_{env} + I_g}{-I_{env} + I_g}. \tag{4.4}$$

A control current I_g should be nearly equal to I_{env} for high SNR [26].

The conventional DAB-based circuit in Fig. 4.1 keeps the voltage swing of V_{in} almost constant with I_g proportional to I_{env}. For example, let the available input range of a log domain filter core be from 450 to 550 mV at a power supply of 0.8 V. When I_{in} is a 10-μA sinusoidal wave, the maximum and the minimum of V_{in} are about 513 and 478 mV from Eq. (4.2), respectively, where parameters are set to realistic values as $n = 1.2$, $U_T = 26$ mV, $I_{bias} = 20$ μA, and $V_b = 0.5$ V. It is also assumed that I_g is twice as much as the envelope current of I_{in}. The voltage swing V_{in} of this case is shown in Fig. 4.2 (a). On the other hand, if a 1.0-μA sinusoidal input current I_{in} and $I_g = 2.0$ μA are applied, V_{in} swings from 406 to 441 mV as shown in Fig. 4.2 (b). Although variation of V_{in} is the same as that in the case of $I_{env} = 10$ μA, a swing range of V_{in} is out of the available input range of the filter core. Therefore, the conventional DAB circuit distorts signals at a low-power supply when I_{env} is small.

$V_{DD} = 0.8$ V, $n = 1.2$, $U_T = 26$ mV, $I_{bias} = 20$ uA, $I_g = 2 I_{env}$
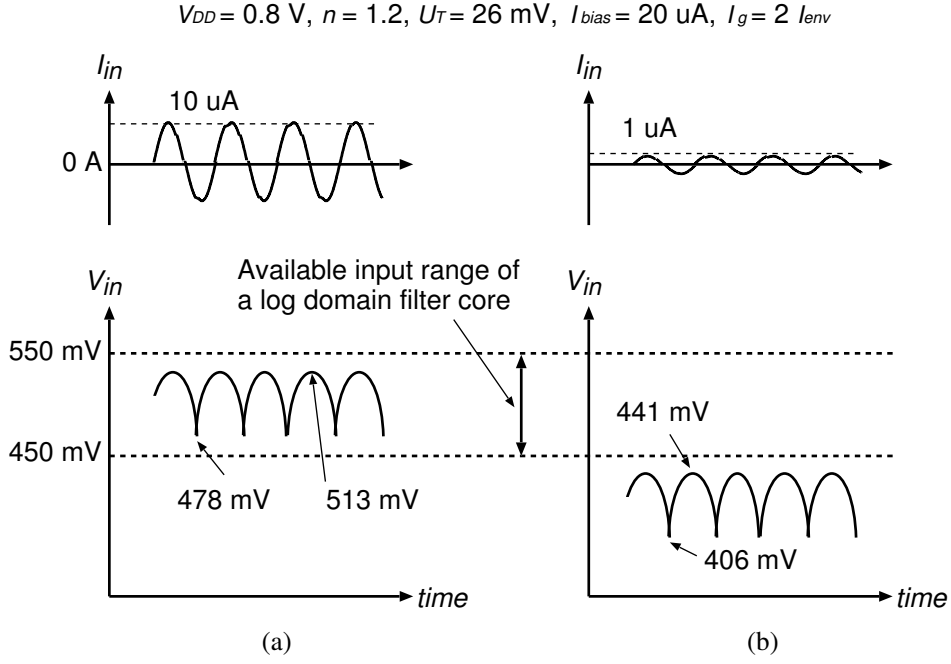
Figure 4.2: Input voltage V_{in} of a log domain filter core and its available input range in conventional DAB-based circuit when (a) I_{in} is a 10-μA sinusoidal current and (b) a 1-μA one.

4.2.2 Proposed Low-Voltage Integrator based on Dynamic Biasing Technique

For low voltage operation, the conventional DAB filter structure is modified. A swing range of V_{in} with I_g varied should be in the narrow input range of a log domain filter core. If the source potential V_s of M_{in} in Fig. 4.1 goes up for small I_g, the voltage swing range illustrated in Fig. 4.2 (b) is lifted up and included in the available input range of the log domain filter core. To enlarge V_s only in the case of small I_g, I_{bias} is replaced with I_g in Fig. 4.1. V_{in} is expressed as

$$V_{in} = nU_T \ln\left(\frac{I_{in} + I_g}{I_g}\right) + V_b. \tag{4.5}$$

Assuming the same parameters with the case of Fig. 4.2, a waveform of V_{in} for $I_{env} = 1.0$ μA becomes the same as that of Fig. 4.2 (a). V_{in} is in the available input range of the filter core even though I_g becomes small, resulting in little output distortion.

One of the simplest example of DAB-based circuits is an integrator. Integrators

(a)

(b)
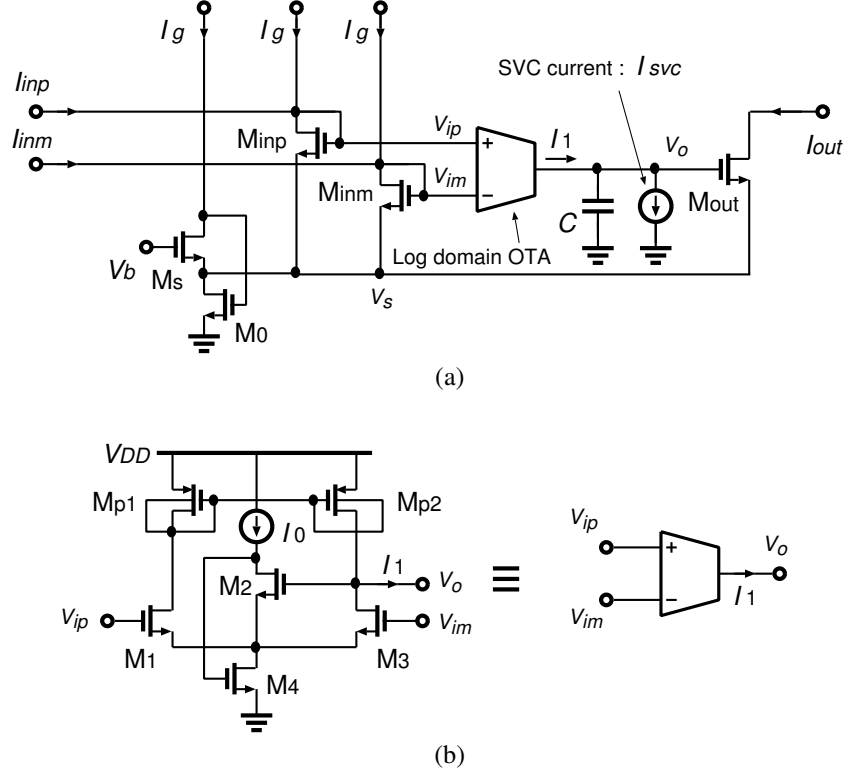
Figure 4.3: Proposed DAB-based integrator.

are often building blocks of a filter and other analog circuits. Its input current I_{in} and output one I_{out} should satisfy

$$\Omega I_{in} = \frac{dI_{out}}{dt} \tag{4.6}$$

where Ω is a unity-gain angular frequency. The low-voltage integrator based on the above proposed technique is shown in Fig. 4.3 (a). Currents I_{inp} and I_{inm} stand for a pair of differential-input currents of an integrator; $I_{inp} - I_{inm} = I_{in}$. V_{ip} and V_{im} excite a log domain OTA the structure of which is illustrated in Fig. 4.3 (b). Each bulk terminal of M_{p1} and M_{p2} is connected to a gate one for low-voltage operation. Little current flows to such a bulk because a bulk-to-source voltage, which is equal to a gate-to-source one, is less than 0.5 V. Relations between gate-to-source voltages and currents of M_1, M_2, and M_3 lead to an output current I_1 of the log domain

OTA [39], [68]

$$I_1 = I_0 \left[\exp \left(\frac{V_{ip} - V_o}{nU_T} \right) - \exp \left(\frac{V_{im} - V_o}{nU_T} \right) \right].$$

(4.7)

Since values of Eq. (4.5) with I_{inp} and I_{inm} substituted for I_{in} are V_{ip} and V_{im}, respectively, and V_o is given by

$$V_o = nU_T \ln \frac{I_{out}}{I_g} + V_b,$$

(4.8)

Eq. (4.7) can be expressed by

$$I_1 = \frac{I_0}{I_{out}} (I_{inp} - I_{inm}) = \frac{I_0 I_{in}}{I_{out}}.$$

(4.9)

A current I_{SVC} is an SVC current, which is needed to keep linearity and time-invariance even if I_g changes. A current flowing into a capacitor is compensated as

$$C \frac{dV_o}{dt} = I_1 - I_{SVC}.$$

(4.10)

From Eqs. (4.6), (4.8), (4.9), and (4.10) an SVC current

$$I_{SVC} = nU_T C \frac{1}{I_g} \frac{dI_g}{dt}$$

(4.11)

must be injected as also presented in Ref. [68] and Ω is given by

$$\Omega = \frac{I_0}{nU_T C}.$$

(4.12)

Optimum design of the control current I_g from the view point of signal to noise plus distortion ratio (SNDR) is provided in Chapter 5.

4.3 State Variable Correction

4.3.1 Current-Type State Variable Correction

A circuit generating an SVC current of Eq. (4.11) is necessary in order to guarantee an ELTI characteristic in the proposed integrator shown in Fig. 4.3. Figure
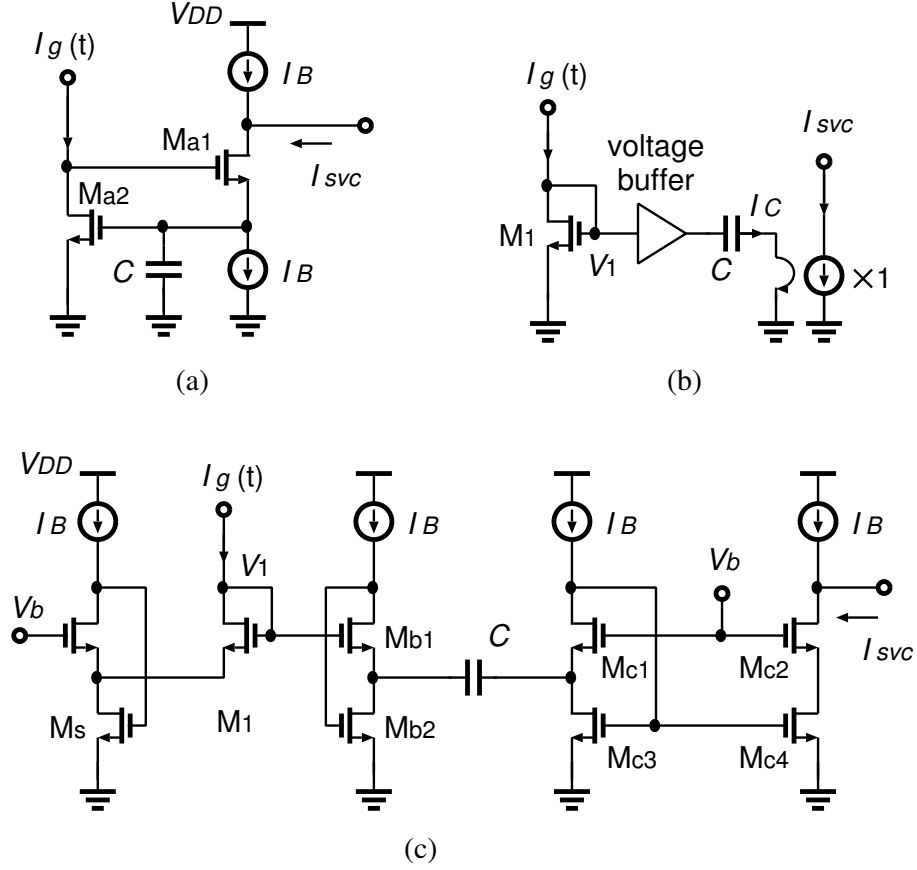
Figure 4.4: State variable correction (SVC) circuits: (a) conventional circuitry, (b) SVC model, and (c) proposed circuitry.

4.4 (a) shows a conventional SVC circuit [59], [68]. A gate potential of M_{a2} becomes $nU_T \ln(I_g/I_S)$ because of a negative feedback configuration composed of M_{a1} and M_{a2}. Therefore a current flowing to the capacitor C equals to Eq. (4.11) and is obtained from a drain terminal of M_{1a}. This circuit is difficult to operate at less than 1.0-V power supply because the sum of gate-to-source voltages of two MOSFETs is larger than 1.0 V.

A proposed SVC circuit employs another scheme shown in Fig. 4.4 (b). A control current I_g is converted to a log-compressed voltage $V_1 = nU_T \ln(I_g/I_S)$ and V_1 is applied to C through a voltage buffer. A current flowing to the capacitor C, which equals a required SVC current expressed as Eq. (4.11), is copied by a current controlled current source. Figure 4.4 (c) shows the proposed configuration where
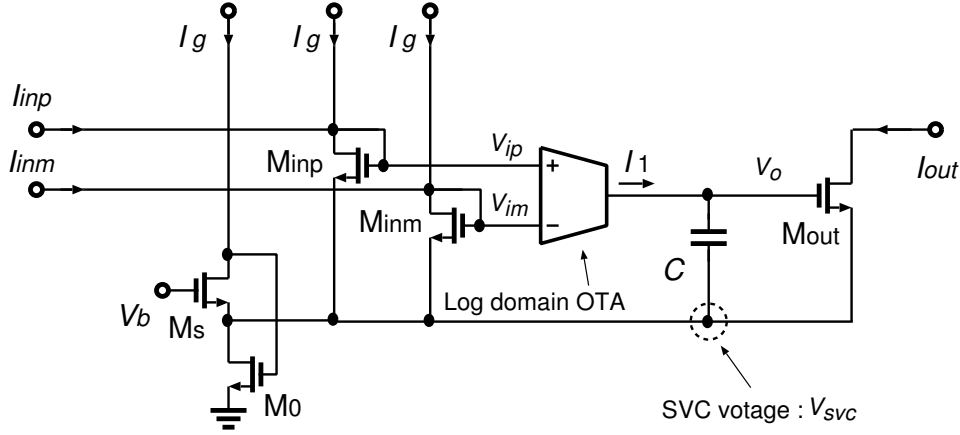
Figure 4.5: Voltage-type SVC method.

MOSFETs M_{b1} and M_{b2} correspond to a voltage buffer and M_{c1} to M_{c4} compose a current mirror circuit as a current controlled current source. The required supply voltage of the proposed SVC circuit equals to the sum of one gate-to-source voltage and two drain-to-source voltages which nearly equals 0.8 V in a 0.35-μm CMOS technology or 0.6 V in a 0.18-μm one.

4.3.2 Voltage-Type State Variable Correction

In Fig. 4.3 (a) a state variable of the integrator for a change of I_g is corrected by a current I_{SVC} which is generated by the SVC circuit shown in Fig. 4.4 (c). Another solution for SVC is to operate a bottom terminal of an integral capacitor C as shown in Fig. 4.5 [69]. In this figure, a voltage V_{SVC} of the terminal is expressed as

$$V_{SVC} = nU_T \ln \left(\frac{I_S}{I_g} \right) + V_b \tag{4.13}$$

and then KCL at a node labeled as V_o leads to

$$C \frac{d}{dt} (V_o - V_{SVC}) = I_0 \left[\exp \left(\frac{V_{ip} - V_o}{nU_T} \right) - \exp \left(\frac{V_{im} - V_o}{nU_T} \right) \right]. \tag{4.14}$$

From Eqs. (4.6), (4.8), (4.9), (4.13), and (4.14) a differential equation of an integrator expressed as Eq. (4.6) is obtained. Since the voltage-type SVC method does not need an SVC current source shown in Fig. 4.4 (c), a circuit scale of a DAB-based integrator becomes smaller than an integrator with the current-type SVC method.

4.4 Design Examples and Simulated Results

This section describes design examples and simulated results of the conventional DAB-based filter [25], [26], the proposed low-voltage one with the current-type SVC circuit [68], and with the voltage-type SVC method [69] as shown in Fig. 4.6. In Fig. 4.6 the filter cores for each filter are designed as $3^{\rm rd}$-order Chebychev and elliptic filters. Therefore total 6 filters are designed and simulated. The simulated results are compared among in the view of dynamic range characteristics under a low-supply voltage. Each of filters in Fig. 4.6 takes a pseudo differential configuration and uses two log domain filter cores. RLC prototype ladder filters of $3^{\rm rd}$-order Chebychev filter with 1-dB passband ripple and elliptic filter with 1-dB passband ripple and 40-dB stopband attenuation from 2.5 Hz are shown in Fig. 4.7 (a) and (b), respectively. According to Appendix A, log domain filter cores for the prototype filters are synthesized by using log domain signal flow graph (SFG) [71] and a log domain summing circuit [92].

The designed filters are simulated assuming a 0.18-μm CMOS process and using a power supply of 0.6 V. It is also assumed in this simulation that a control circuit ideally generates a control current I_g: $I_g = \alpha I_{env}$ where a coefficient α is 3 and I_{env} is an envelope current of an input I_{in}.

4.4.1 Conventional Syllabic Companding Log Domain Filter

Figure 4.8 (a) shows a $3^{\rm rd}$-order Chebychev low-pass log domain filter core for the conventional DAB-based filter shown in Fig. 4.6 (a), which is synthesized by use of log domain integrator cores shown in Fig. 4.3 (b) and capacitors C_1 to C_3 as described in Appendix A. On the other hand, a $3^{\rm rd}$-order elliptic low-pass log domain filter core is shown in Fig. 4.8 (b), in which the log domain integrator cores, the capacitors C_4 to C_6, and log domain summing circuits are used [92]. An SVC is not needed in a conventional DAB filter because a control current I_g does not affect to its output

(a)

(b)

(c)
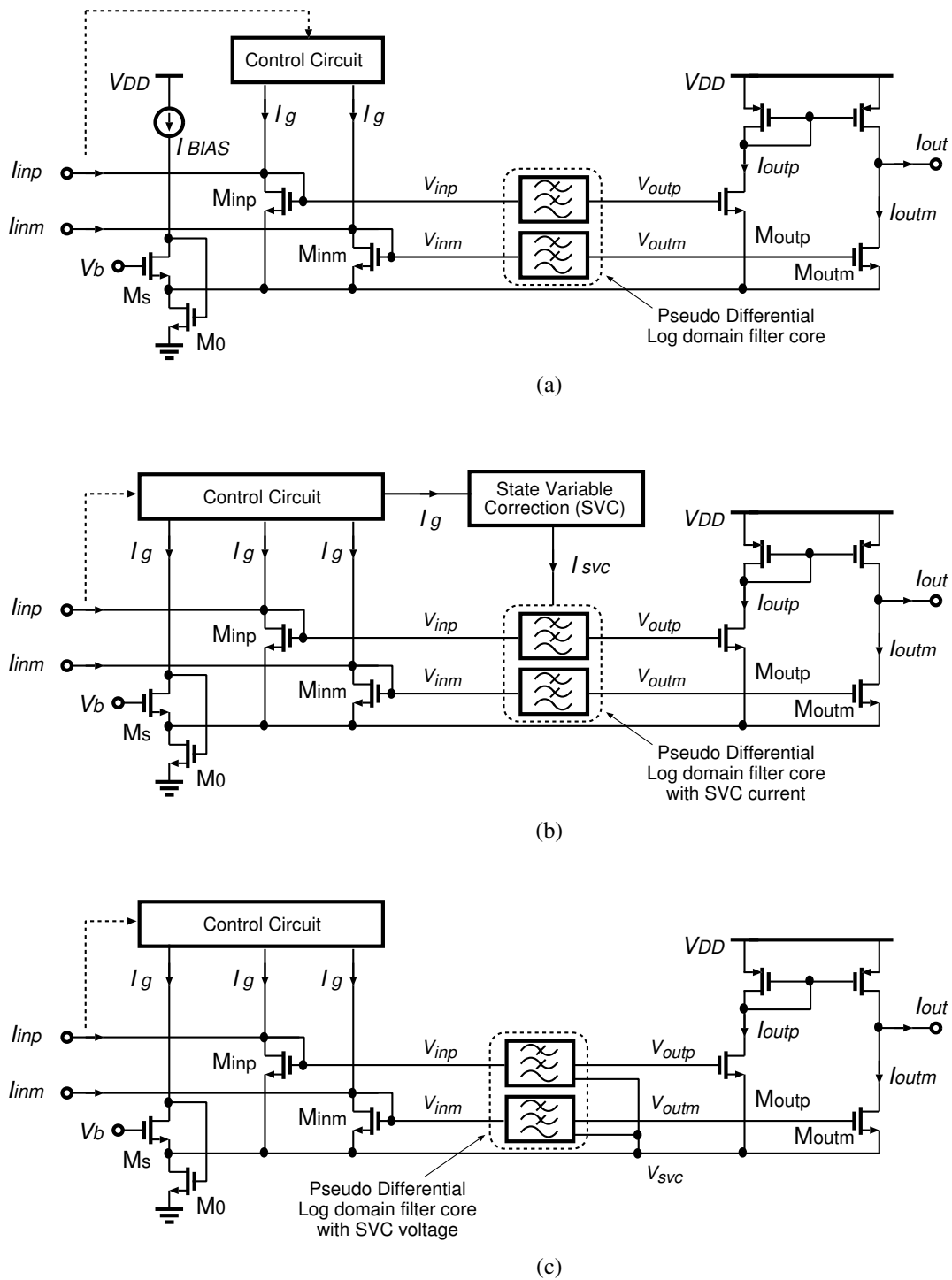
Figure 4.6: The overall syllabic companding log domain filters using (a) conventional dynamically adjustable biasing (DAB) technique, (b) proposed low-voltage DAB technique with current-type SVC, and (c) with voltage-type SVC.
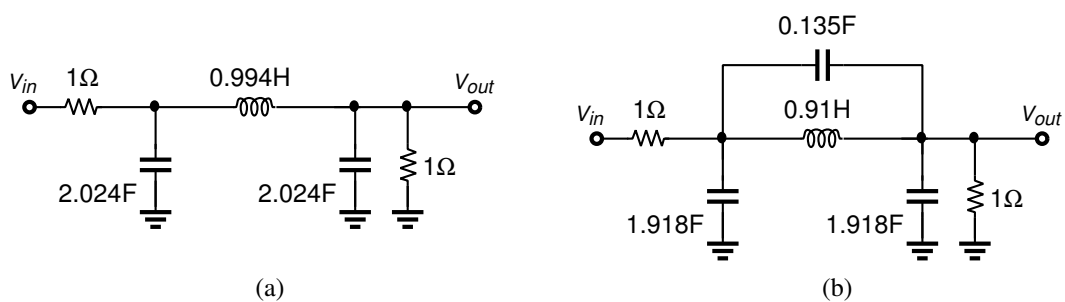
Figure 4.7: RLC prototype ladders: (a) 3rd-order Chebychev filter with 1-dB passband ripple and (b) 3rd-order elliptic filter with 1-dB passband ripple and 40-dB stopband attenuation from 2.5 Hz.
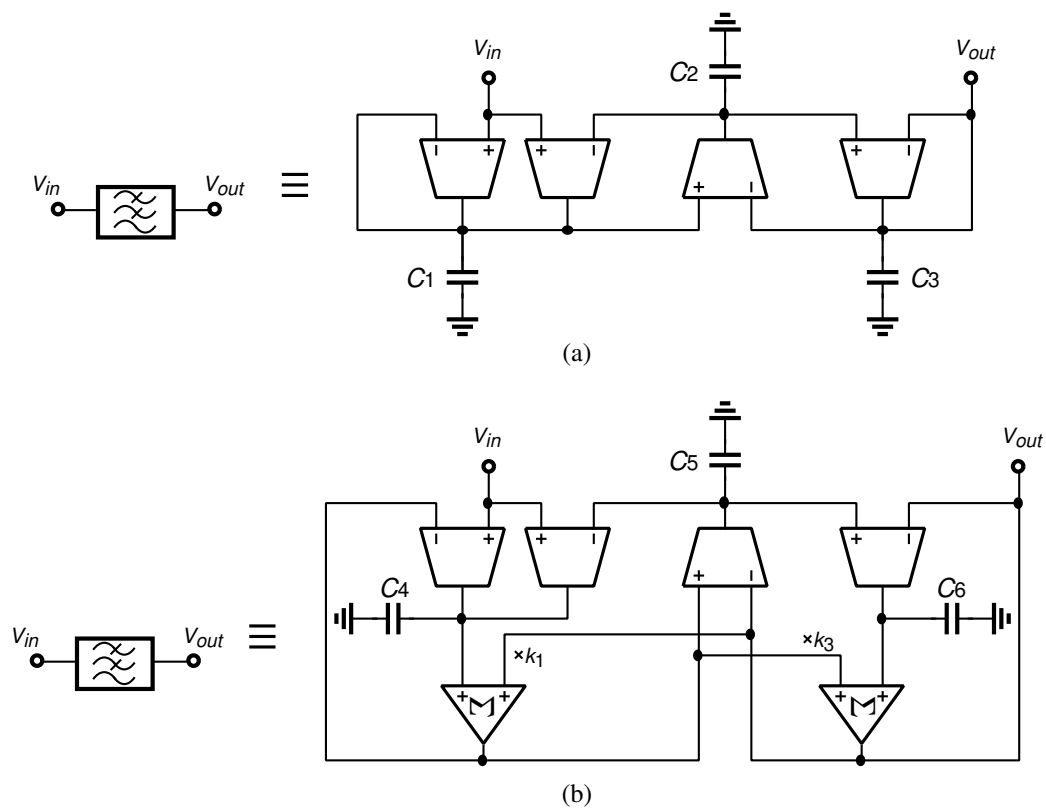
Figure 4.8: Log domain filter cores for the conventional DAB-based filters: (a) 3rd-order Chebychev (all pole) low-pass filter and (b) 3rd-order elliptic (with transmission zeros) low-pass filter.
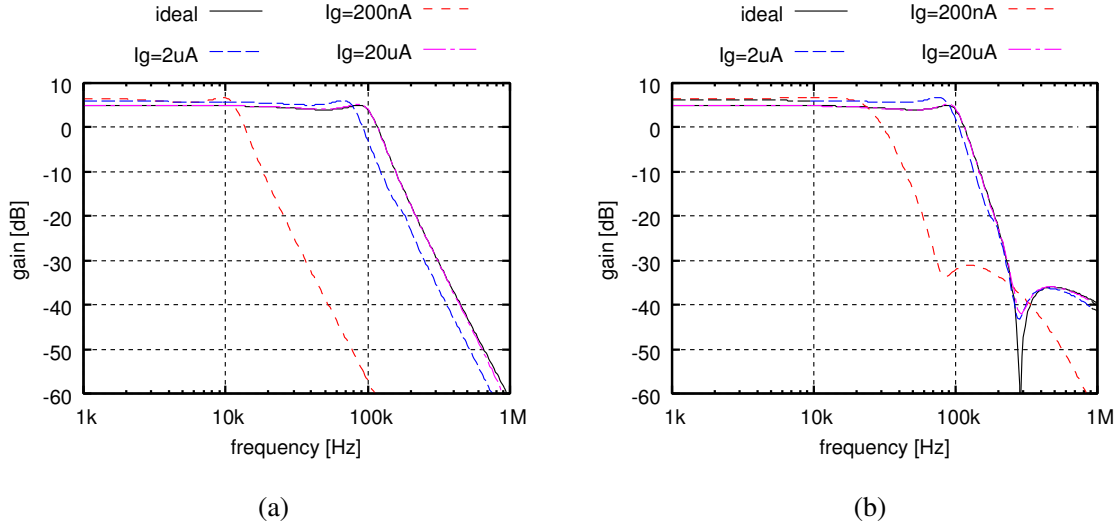
Figure 4.9: Frequency response of the conventional DAB-based filters: (a) 3rd-order Chebychev filter and (b) 3rd-order elliptic filter.

current I_{out} [26]. A transconductance G_m of log domain OTAs is expressed as

$$G_m = \frac{I_0}{nU_T}. \tag{4.15}$$

When all the transconductances are 51.0 μS for a 100-kHz cutoff frequency f_c, the capacitances $C_1 = C_3$ and C_2 in Fig. 4.8 (a) become 161.1 pF and 79.1 pF, respectively, while the capacitances $C_4 = C_6$, C_5, and a coefficient $k_1 = k_3$ in Fig. 4.8 (b) are 163.3 pF, 72.4 pF, and 0.0657, respectively.

Simulated frequency responses of the filters for different I_g's is shown in Fig. 4.9. It is confirmed that f_c's of the both filters decrease as I_g becomes small. This is because a voltage swing of an input of a log domain filter core is out of an available input range of the filter core for a small input current as shown in Fig. 4.2. It decreases a drain-to-source voltage of MOSFET M_4 in the first stage log domain OTA shown in Fig. 4.3 (b) of the filter core, and then a p-channel MOSFET as a current source I_0 is not in a saturation region.

The upper-side graphs of Figs. 4.10 (a) and (b) show the magnitude of the fundamental components of the output current I_{out}, the total harmonic distortion (THD), and the output current noise I_{on}, where a 100-kHz sinusoidal input current
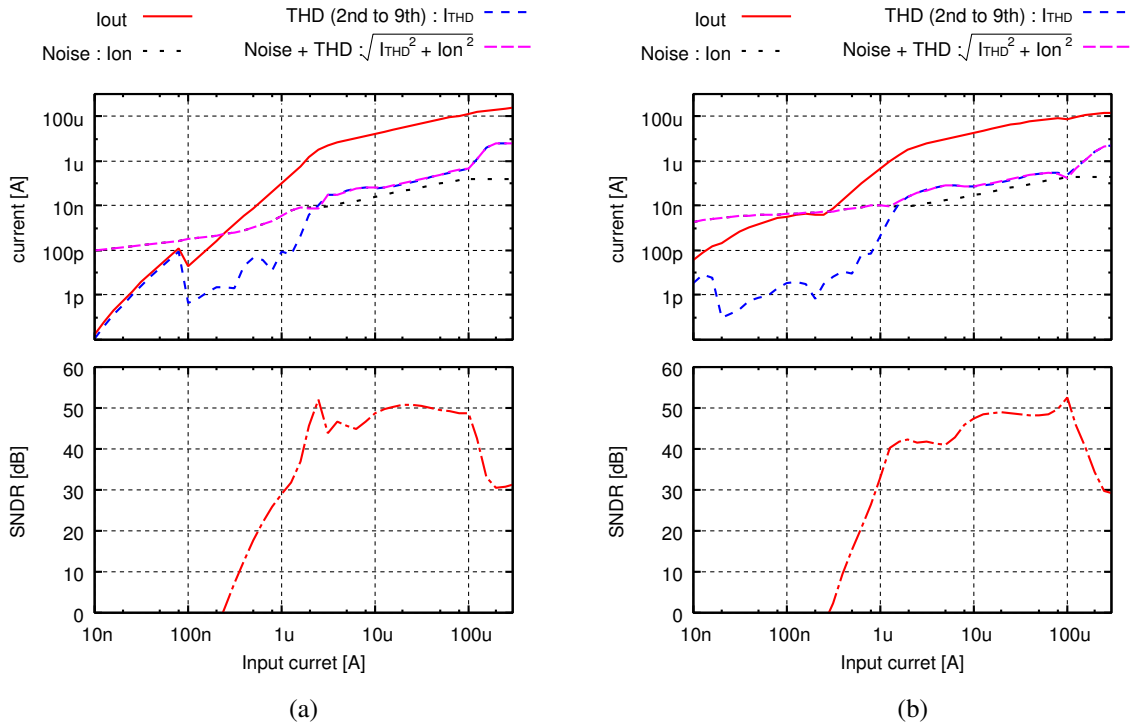
Figure 4.10: Dynamic range characteristics at a 100-kHz tone for the conventional DAB-based filters: (a) 3rd-order Chebychev filter and (b) 3rd-order elliptic filter.

I_{in} is applied. The plots of the fundamental magnitude are simply denoted as "I_{out}" and the THD I_{THD} is defined as the square-root of sum of squires of the second to the ninth harmonic components in the sense of RMS. The noise I_{on} is calculated from an average output noise currents during one period of a sinusoidal input. In addition the noise plus distortion components calculated from $\sqrt{I_{THD}^2 + I_{on}^2}$ are also shown in the same figures. In this figures, the fundamental components I_{out} of the both filters begin to decrease when I_{in} is nearly equal to 2 μA. This is consistent with the results shown in Fig. 4.9 where the cutoff frequencies of the filters begin to decrease when $I_g = 2.0$ μA. The signal-to-noise-plus-distortion ratios (SNDRs) for the filters are shown in the lower-side graphs of Fig. 4.10, which are obtained by using results in the upper-side graph of Fig. 4.10 and

$$\mathrm{SNDR} = 10 \log \frac{I_{out}^2}{I_{on}^2 + I_{THD}^2} \quad [\mathrm{dB}]. \tag{4.16}$$

It is confirmed that the SNDRs of the both filters decrease for a small input current
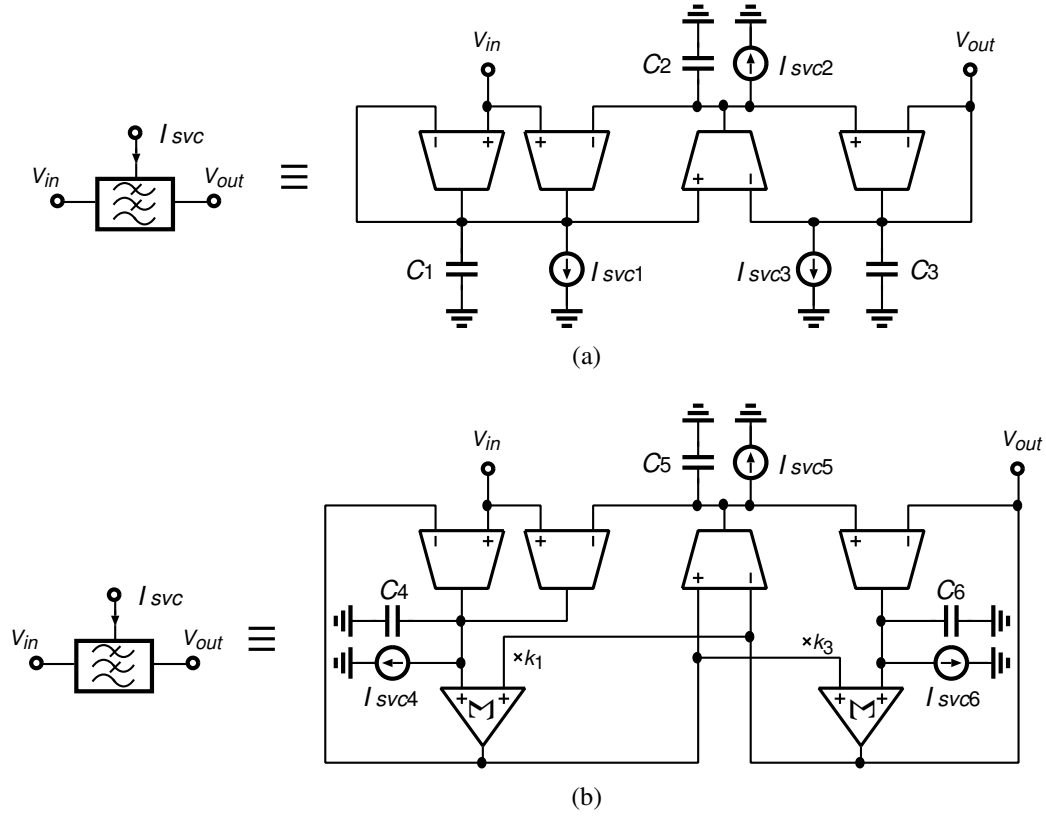
Figure 4.11: Log domain filter cores for the proposed low-voltage DAB-based filters using current-type SVC: (a) 3rd-order Chebychev (all pole) low-pass filter and (b) 3rd-order elliptic (with transmission zeros) low-pass filter.

and thus the dynamic ranges (DRs), which are defined as

$$\text{DR} = 20 \log \frac{I_{out,max}}{I_{on}}, \tag{4.17}$$

become narrow under low-supply voltage where $I_{out,max}$ means a 40-dB ratio of an output signal to THD.

4.4.2 Proposed Syllabic Companding Log Domain Filter Using Current-Type State Variable Correction

Figure 4.11 (a) and (b) show a 3rd-order Chebychev filter core and an elliptic one, respectively, for the proposed DAB-based filter in Fig. 4.6 (b). For SVC the current sources $I_{SVCi} = nU_T C_i I'_g / I_g$ $(i = 1, \dots, 6)$ can be used for higher-order
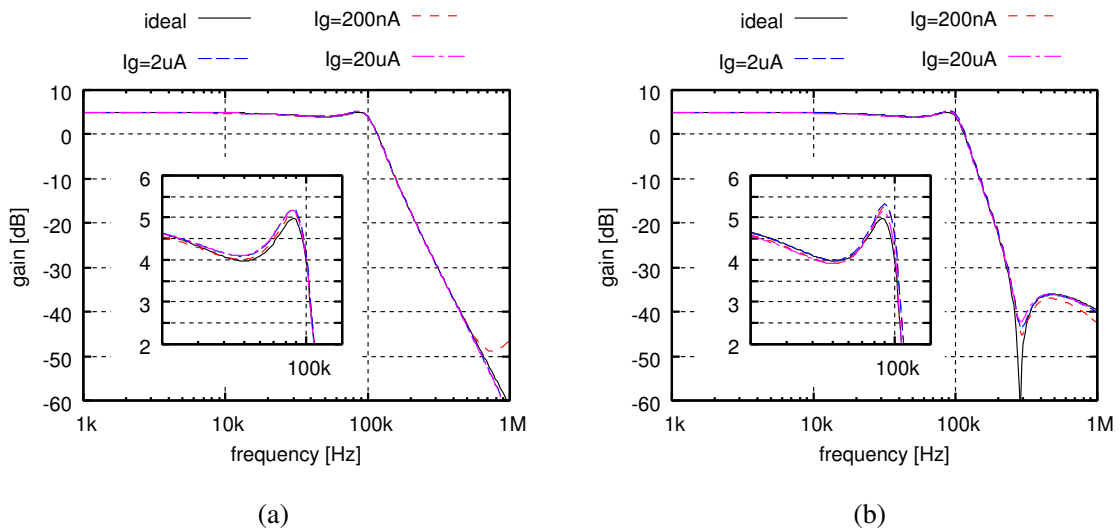
Figure 4.12: Frequency response of the proposed DAB-based filters using current-type SVC: (a) 3rd-order Chebychev filter and (b) 3rd-order elliptic filter.

filters as described in Appendix A and located in parallel with each capacitor, C_1 to C_6. The currents I_{SVCi}'s are generated from the proposed low-voltage SVC circuit shown in Fig. 4.4. The values, such as transconductances and capacitances, of the filters are the same as the conventional DAB-based filters.

Figure 4.12 shows frequency response of the proposed DAB-based filters for different control currents I_g's. Although the passband ripples are slightly larger than 1 dB, the passband gain and the cutoff frequency are well matched regardless of change of I_g because the proposed DAB technique keeps a bias voltage of an input of a filter core constant and makes the core operating normally under low-supply voltage.

Dynamic characteristics of the filters are shown in Fig. 4.13. The fundamental output currents I_{out}'s of the both filters maintain the gradient constant when I_{in} is less than 2.0 μA, and thus the SNDRs become large compared to the conventional DAB-based filters for a small I_{in}. Since the input current for SNDR = 0 dB becomes about two decades lower than the conventional one, the DRs expressed as Eq. (4.17) are also extended. The SNDRs for $I_{in} < 10$ nA drastically decrease because low control current I_g degrades a bandwidth of the filters and thus the fundamentals
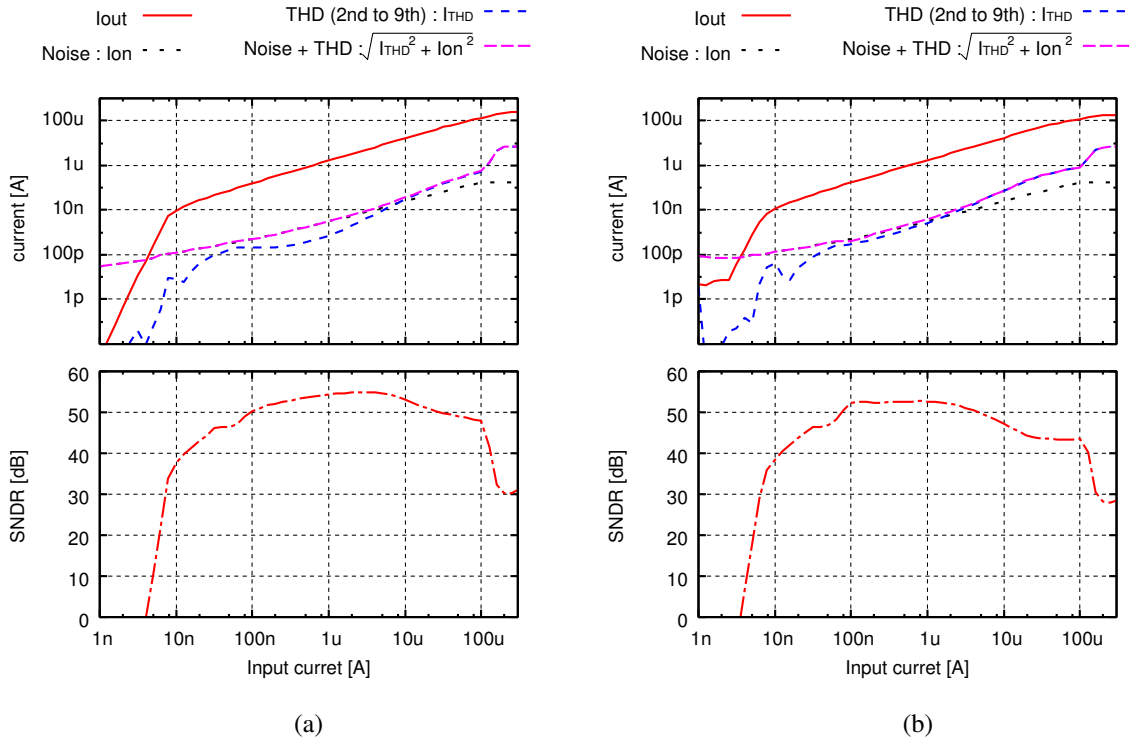
Figure 4.13: Dynamic range characteristics at a 100-kHz tone for the proposed DAB-based filters using current-type SVC: (a) $3^{\rm rd}$-order Chebychev filter and (b) $3^{\rm rd}$-order elliptic filter.

become small near the cutoff frequency.

In order to verify operation of an SVC circuit, transient simulations are performed by applying an input current to the filters, the envelope of which changes as shown in Fig. 4.14. A control current I_g for the input is three times as large as the envelope. Figure 4.15 shows output currents of the filters where they are expanded in a time scale. In this figure it is confirmed that the output waveforms of the filters with SVC current sources approach an ideal response, which is an output of a ladder filter, rather than the filters without SVC. Therefore state variables of the filters are corrected by the SVC circuit shown in Fig. 4.4 (c).
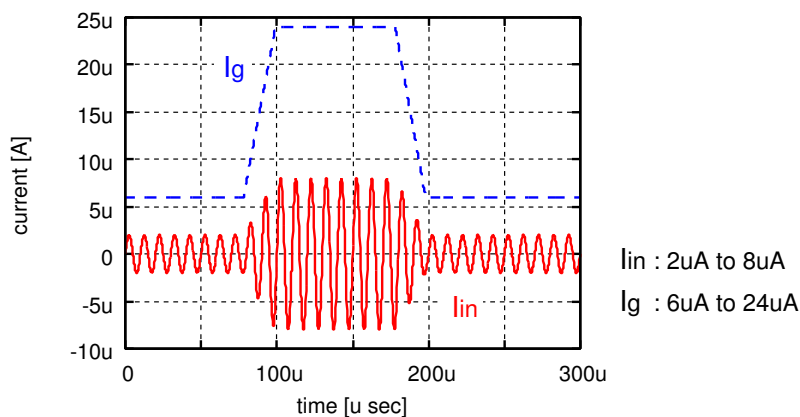
Figure 4.14: Input current I_{in} and a control current I_g for transient simulations.
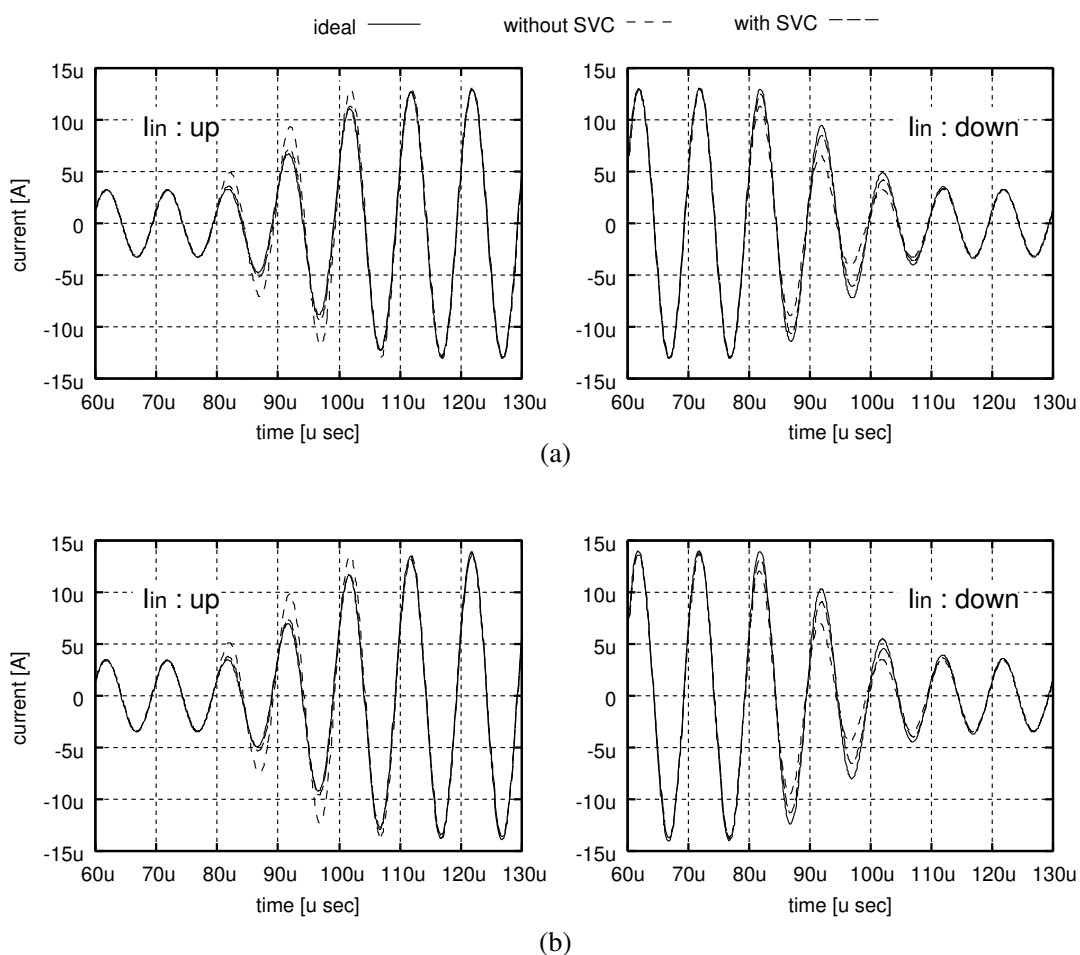
Figure 4.15: Output current I_{out} when the envelope changes: (a) Chebychev filter and (b) elliptic filter.
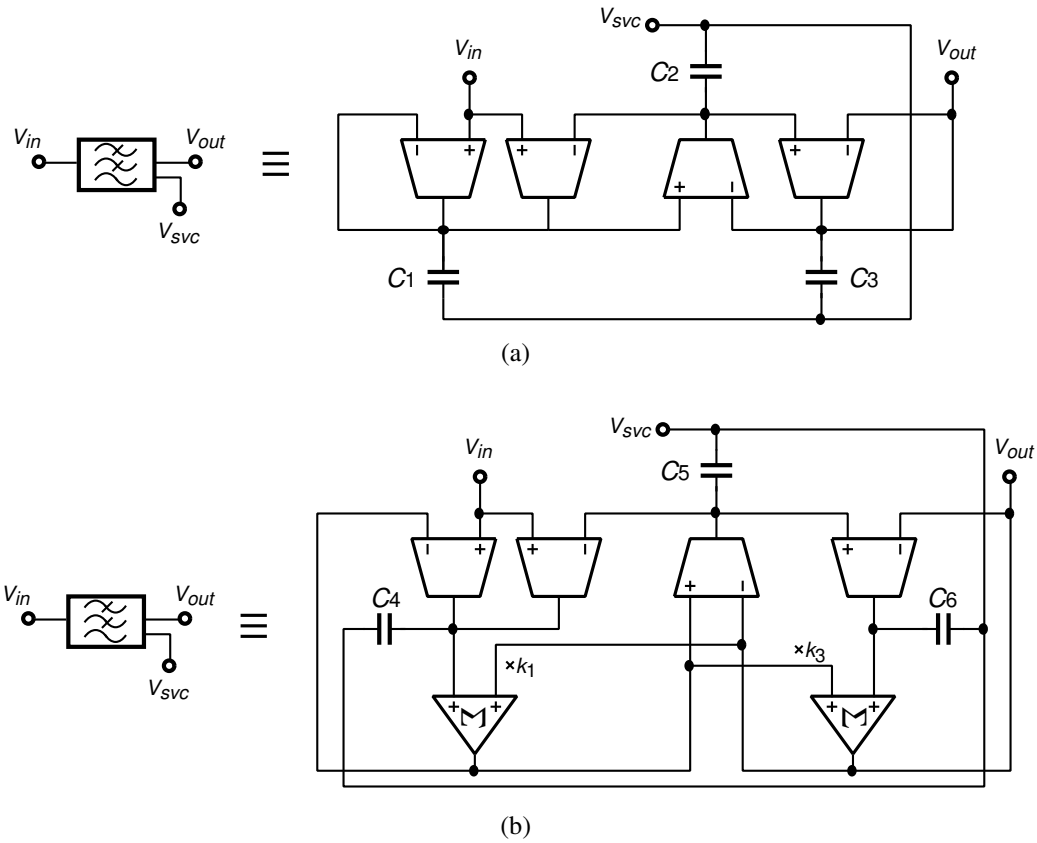
Figure 4.16: Log domain filter cores for the proposed low-voltage DAB-based filters using voltage-type SVC: (a) 3rd-order Chebychev (all pole) low-pass filter and (b) 3rd-order elliptic (with transmission zeros) low-pass filter.

4.4.3 Proposed Syllabic Companding Log Domain Filter Using Voltage-Type State Variable Correction

Figure 4.16 shows 3rd-order Chebychev and elliptic log domain filter cores for the proposed DAB filters using voltage-type SVC shown in Fig. 4.6 (c). According to Appendix A, the one sides of the terminals of the capacitors, C_1 to C_6, are connected to a drain of MOSFET M_0 for SVC. The capacitances and transconductances of log domain OTAs are the same as above filter cores shown in Figs. 4.11 and 4.16.

Frequency responses of the filters for different I_g's are shown in Fig. 4.17. These responses and a location of zero in the elliptic filter correspond to an ideal one except for slightly large passband ripple. Figure 4.18 shows dynamic characteristics for a
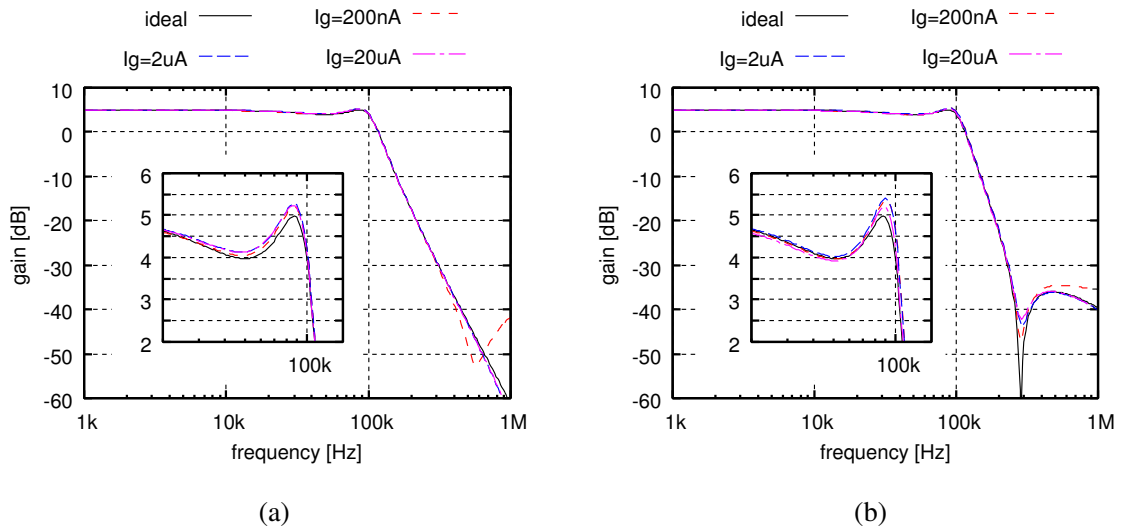
Figure 4.17: Frequency response of the proposed DAB-based filters using voltage-type SVC: (a) 3rd-order Chebychev filter and (b) 3rd-order elliptic filter.
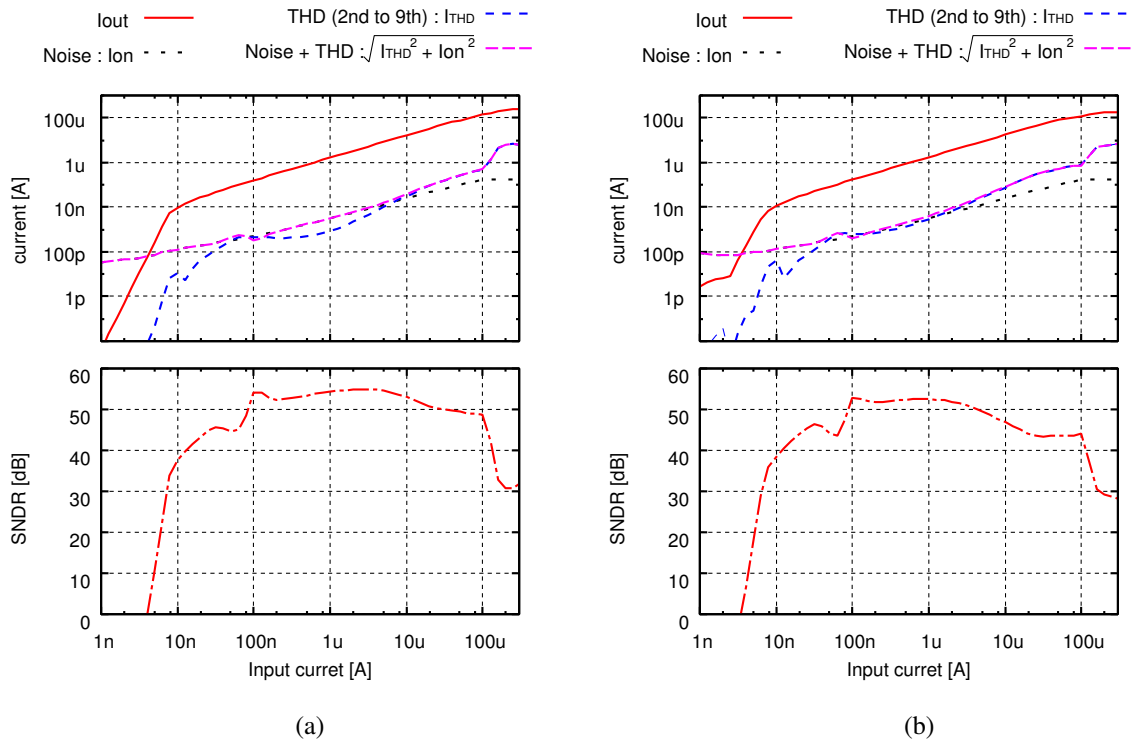
Figure 4.18: Dynamic range characteristics at a 100-kHz tone for the proposed DAB-based filters using voltage-type SVC: (a) 3rd-order Chebychev filter and (b) 3rd-order elliptic filter.
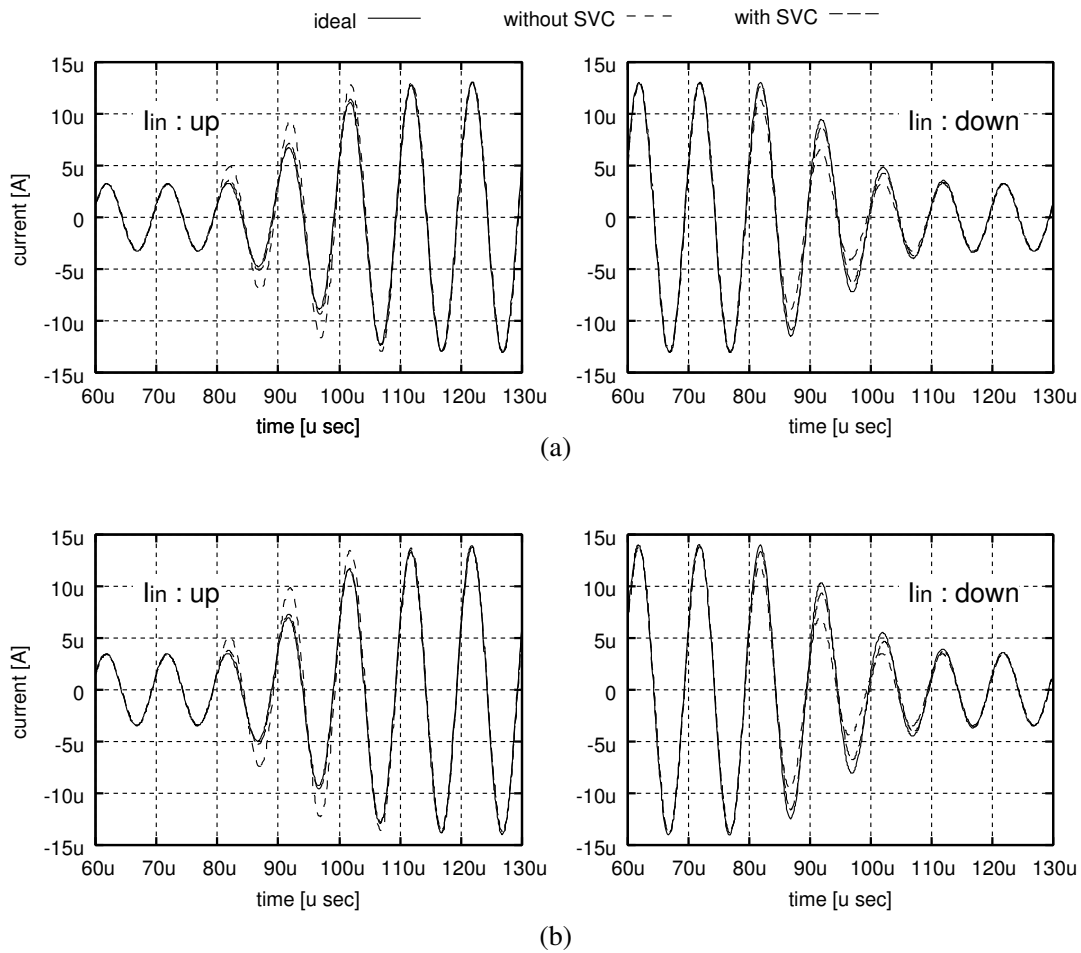
Figure 4.19: Output current I_{out} when the envelope changes: (a) Chebychev filter and (b) elliptic filter.

100-kHz sinusoidal input current. It is confirmed that DRs of the filters are extended by the proposed DAB technique. The output current waveforms are shown in Fig. 4.19 where an input current I_{in} and a control current I_g shown in Fig. 4.14 are applied to the filters. It is verified that the filters have an ELTI relation between the input and the output because the waveforms, which are output of the filters using SVC, approach that of the ideal waveforms.

4.4.4 Comparison of Two State Variable Correction Methods

The proposed two SVC methods have different characteristics in terms of simplicity and accuracy. Since the current-type SVC circuit shown in Fig. 4.4 (c) needs a capacitor and several MOSFETs, the voltage-type SVC method has a considerable area efficiency compared to the current-type one. However, since log domain filter cores in a DAB-based filter with the voltage-type one need floating capacitors on the signal path, a parasitic capacitance C_{par} of the capacitors between the bottom terminals and substrate would be observed. Furthermore, a finite impedance r_o at the drain terminal of MOSFET M_0 in Fig. 4.5 and the capacitance C_{par} form a time-variant time constant depending on change of I_g because the impedance r_o is expressed as

$$r_o = \frac{\lambda_{WS}(nU_T)^2}{5I_g} \tag{4.18}$$

where λ_{WS} means a coefficient which is inversely proportional to the channel length of M_S in Fig. 4.5. The fact leads to the following differential equation:

$$\frac{1}{r_o}\left\{\left(nU_T\ln\frac{I_S}{I_g} + V_b\right) - \hat{V}_{SVC}\right\} = C_{par}\frac{d}{dt}\hat{V}_{SVC} \tag{4.19}$$

and, the voltage $\hat{V}_{SVC}$ derived from this equation is therefore employed as an SVC voltage instead of V_{SVC} in Fig. 4.5 and induce an SVC error for the output current I_{out}. In this case, it is impossible to correct the error because the voltage-type SVC method is realized by only connection of terminals as shown in Fig. 4.5.

On the other hand, the current-type SVC circuit in Fig. 4.4 (c) has no time-varying time constant due to change of I_g because bias currents of each MOSFET is almost constant apart from M_1. If an amplitude SVC current error is observed in simulation results, one can easily adjust the aspect ratios of the current mirror MOSFETs, M_{c1} to M_{c4}, to reduce the error. Therefore it can be said that the voltage-type SVC method provides area efficacy, while the current-type one can generate an accurate SVC signal I_{SVC}, and thus they can be used as situation demands.

4.5   Conclusion

The technique to achieve wide dynamic range of analog filters under a low-supply voltage has been presented by using dynamically adjustable biasing. For an externally linear time-invariant relation of a filter, the low-voltage state variable correction methods have been also proposed. The techniques is applicable to any log domain filters, such as all-pole filters and filters with transmission zeros. The effectiveness of the proposed technique is confirmed through simulated results of Chebychev and elliptic filters.

Chapter 5

Optimum Design Method of Control Current for Dynamic Range

5.1   Introduction

Syllabic companding log domain filters, or dynamically adjustable biasing (DAB) filters, require a control current to achieve wide dynamic range. In the conventional filters, about double value of an envelope of an input current has been empirically used for the control current [26]. While a large control current suppresses a voltage swing of internal nodes in the filters to decrease distortion under a low supply voltage, a small one is preferable for small output noise. This means that there is an optimum control current corresponding to each input signal amplitude. In this chapter an optimum design method of a control current is described from the viewpoint of enhancing a signal-to-noise-plus-distortion ratio (SNDR) of a low-voltage DAB-based filter. First, for saving the design time, a filter is approximately analyzed, resulting in its SNDR as a function of an input current amplitude and a control current. It is not needed to calculate the third-order intermodulated distortion and SNDR for all combination of an input current and a control one from SPICE simulation results. Next, finding a locus of the control current for the input through a peak SNDR, an optimum control current can be obtained theoretically. In the last section, a design example is described for a third-order DAB-based Butterworth low-pass filter and results of a theoretical optimum control current and a simulated one are compared.

5.2   Noise and Distortion Modeling

5.2.1   Noise Analysis

Figure 5.1 (a) shows the low-voltage syllabic companding log domain filter in which a circuit for a state variable correction is ignored. Since internal voltages of a companding circuit behave in non-linear manner for an input current, its output noise is amplitude-modulated by the input and thus a small signal model cannot be used for obtaining an exact output noise [70]–[73]. However, in the DAB-based filters as shown in Fig. 5.1 (a), a noise due to a control current I_g is rather dominant than the amplitude-modulated noise. Therefore a small signal model shown in Fig. 5.1 (b) is used for noise analysis.

In Fig. 5.1 (b) an input-referred equivalent noise voltage power spectrum density (PSD) of MOSFETs M_i $(i = 0, 1, \ldots, 5)$ is expressed as

$$\overline{v_{nib}^2} = 4kT\frac{2}{3}\frac{1}{g_{mi}} \ (i = 0, 1, \ldots, 5) \tag{5.1}$$

where a flicker noise is ignored and a long-channel length is assumed [2]. Values named as h_1 and h_2 are a DC gain of the log domain filter core, and noise voltages $\overline{v_{nf1}^2}$ and $\overline{v_{nf2}^2}$ are an input-referred equivalent noise voltage PSD of the filter core. Note that $\overline{v_{nf1}^2}$ and $\overline{v_{nf2}^2}$ are independent of a control current I_g because an operating point of the filter core is not changed by I_g: the noise voltages are constant value. As a consequence, from the superposition principle of power at the output $I_{outp} - I_{outm}$ an output noise current $\overline{I_{out,noise}^2}$ is obtained as

$$\overline{I_{out,noise}^2} = \frac{16}{3}kTg_{m4}^2 \left(\frac{|h_1|^2}{g_{m1}} + \frac{1}{g_{m4}}\right) + 2g_{m4}^2|h_1|^2\overline{v_{nf1}^2}$$

where $g_{m1} = g_{m2}$, $g_{m4} = g_{m5}$, and $h_1 = h_2$. In this case assuming that an aspect ratio of MOSFETs M_i $(i = 1, 2, 4, 5)$ is the same as each other, its drain currents also become identical and thus $g_{m1} = g_{m2} = g_{m4} = g_{m5}$. The transconductances g_{mi}'s $(i = 1, 2, 4, 5)$ are given as

$$g_{mi} = \frac{\partial I_g}{\partial V_{gs}} = \frac{I_g}{nUT} \ (i = 1, 2, 4, 5) \tag{5.2}$$

(a)

(b)
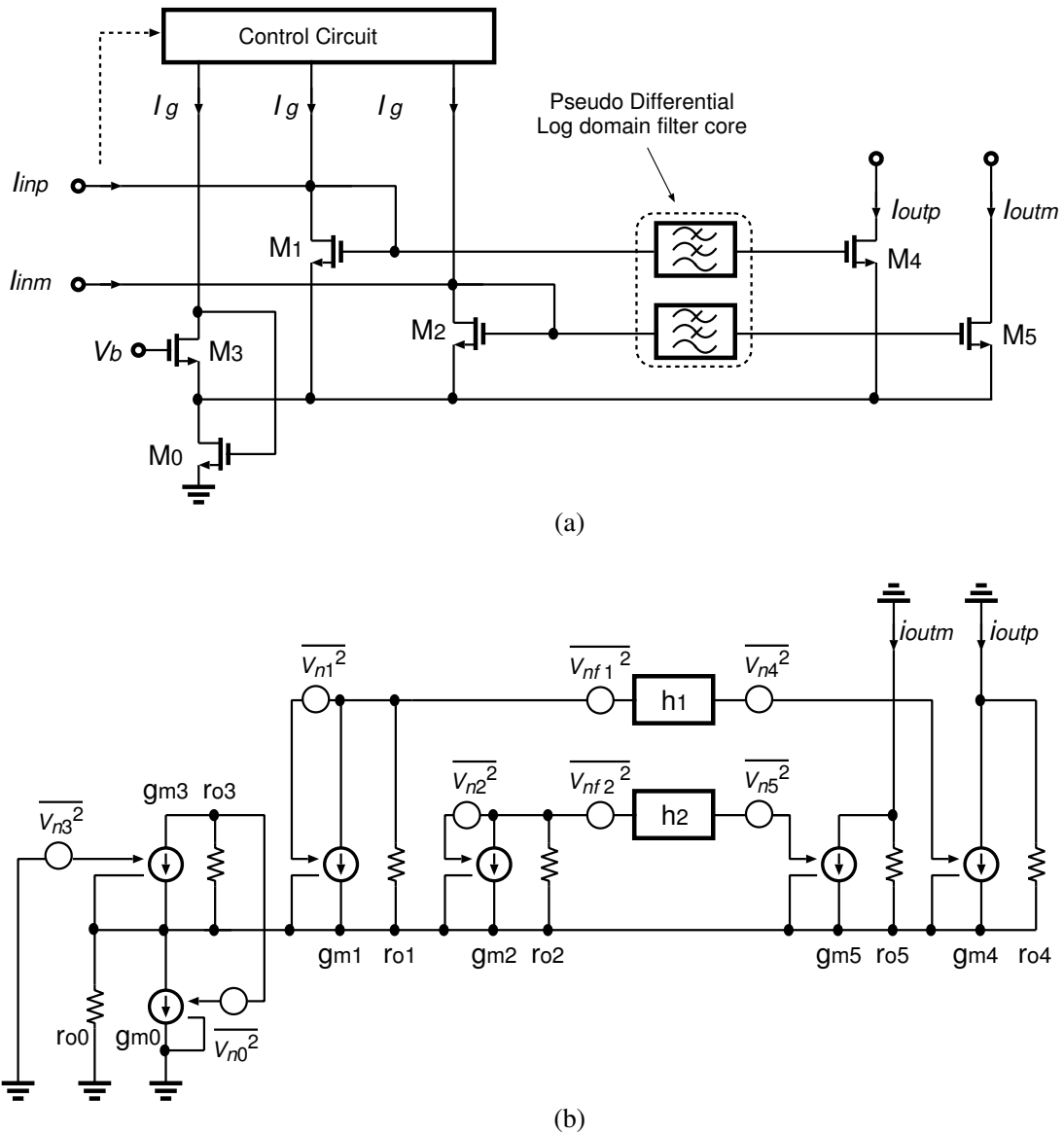
Figure 5.1: Low-voltage syllabic companding log domain filter (DAB-based filter): (a) circuitry and (b) small signal model for noise analysis.

and thus, the output current noise PSD

$$\overline{I^2_{out,noise}} = \frac{32}{3}kT\frac{I_g}{nU_T} + 2\left(\frac{I_g}{nU_T}\right)^2 \overline{v^2_{nf1}} \ \ [\text{A}^2/\text{Hz}] \tag{5.3}$$

is given, which is a function of a control current I_g.

5.2.2 Distortion Model

For a true optimum design of syllabic companding filters a decision of capacitances and small signal transconductances of a log domain filter core must be considered for reducing its distortion and noise. In this case the optimum parameters would be determined by transforming state variables of the filter core into non-linear ones and then applying methods described in Refs. [74],[75]. However, since a non-linearity for change of I_g is only considered, an optimum design of the parameters in the filter core is not analytically taken into account in this chapter. In other words a distortion of a syllabic companding filter is approximately modeled from its DC characteristics. Letting a DC offset and a second-order distortion be ignored and a third-order one be dominant, an output current of the filter is expressed as

$$I_{out} = \alpha I_{in} + \beta I_{in}^3 \tag{5.4}$$

where α and β mean a DC gain and a coefficient of the third-order distortion, respectively. Note that β is varied by I_g: the greater I_g is, the smaller the distortion becomes, or small $|\beta|$, because a distortion at MOSFETs M_1 and M_2 in Fig. 5.1 (a) decreases for a large input current. Obtaining DC characteristics for each I_g from simulations, α and β are given by the least square method (LSM) for the characteristics. Eventually, the obtained relations of I_g-α and I_g-β lead to following approximated functions for I_g:

$$\alpha(I_g) = \alpha_0 + \alpha_1 \left(\log \frac{I_g}{1 \text{ A}} \right) + \alpha_3 \left(\log \frac{I_g}{1 \text{ A}} \right)^2 + \ldots = \sum_{i=0}^{\infty} \alpha_i \left(\log \frac{I_g}{1 \text{ A}} \right)^i \tag{5.5}$$

$$\beta(I_g) = \frac{\beta_2}{I_g^2} \tag{5.6}$$

in which the coefficients, α_i ($i = 0, 1, 2, \ldots$) and β_2, are fitted by use of the LSM again.

In this optimum design a third-order intermodulated distortion (IMD$_3$) is considered for SNDR as an evaluation function. Letting two tones with the same amplitude and different angular frequency, $I_i \cos \omega_1 t$ and $I_i \cos \omega_2 t$, be applied to the filter expressed by Eqs. (5.5) and (5.6), an output includes not only a fundamental tones

$I_{out,\text{fund.}}$ with desired angular frequency ω_1 and ω_2 but also IMD$_3$ components $I_{out,\text{IMD3}}$ with $2\omega_1 - \omega_2$ and $2\omega_2 - \omega_1$ [76], where

$$I_{out,\text{fund.}} = \left(\alpha(I_g) + \beta_2 \frac{9}{4} \frac{I_i^2}{I_g^2} \right) I_i \tag{5.7}$$

$$I_{out,\text{IMD3}} = \frac{3}{4} |\beta_2| \frac{I_i^3}{I_g^2}. \tag{5.8}$$

5.2.3 SNDR and Boundary Condition of Control Current

From the output noise current $\overline{I_{out,noise}^2}$, the fundamental output current $I_{out,\text{fund.}}$, and the output distortion $I_{out,\text{IMD3}}$, which are expressed as Eqs. (5.3), (5.7), and (5.8), respectively, an SNDR of the filter as a function of a control current I_g and an input current amplitude I_i can be obtained as

$$\text{SNDR} = 20 \log \frac{I_{out,\text{fund.}}}{\sqrt{2 f_{NBW} \overline{I_{out,noise}^2} + I_{out,\text{IMD3}}^2}} \tag{5.9}$$

where f_{NBW} is an equivalent noise bandwidth of the filter.

Although an arbitrary value can be theoretically taken for I_g, in practice, I_g has a lower limit $I_{g,min}$ and a upper limit $I_{g,max}$. The former is determined whether a frequency response of the filter is influenced by small I_g or not. In other words, since a undesired bandwidth degradation of the filter causes due to relative large parasitic capacitances of MOSFETs M_0 to M_5 in Fig. 5.1 (a) for its drain currents I_g's, the smallest control current which still makes a varied frequency response of the filter must be used as $I_{g,min}$. On the other hand, the latter is chosen as long as all MOSFETs in Fig. 5.1 (a) are biased in a weak inversion region, not a strong inversion one.

As a result, the optimum control current I_g would be obtained by finding a locus of I_g, which almost maximizes SNDR expressed in Eq. (5.9) for I_i, under the boundary condition, $I_{g,min} \leq I_g \leq I_{g,max}$. One solution for the problem, a value J given by

$$
\begin{aligned}
J &= \int_{I_{g,min}}^{I_{g,max}} \text{SNDR}(I_i, I_g) dI_g \\
&= \int_{I_{i,min}}^{I_{i,max}} f(I_i, I_g, I_g') dI_i
\end{aligned}
\tag{5.10}
$$

is considered as a variation problem to let J be an extremal value, where

$$f(I_i, I_g, I'_g) = \text{SNDR}(I_i, I_g) \frac{dI_g}{dI_i}. \tag{5.11}$$

In this case $I_g(I_i)$ can be obtained by using Euler's differential equation expressed as

$$\frac{d}{dI_i} \left(\frac{\partial f}{\partial I'_g} \right) - \frac{\partial f}{\partial I_g} = 0 \tag{5.12}$$

and solving Eq. (5.12) for I_g. However one cannot solve for $I_g(I_i)$ in algebraic form by using any formula because Eq. (5.12) results in an equation more than fifth order. Another solution is to use a numerically method. If it is assumed that $I_g(I_i)$ is a monotone increasing function for the boundary condition $I_{g,min} \leq I_g \leq I_{g,max}$, the optimum control current can be obtained by finding peak SNDRs for all combinations of I_g and I_i. Since this method is valid in practice, utilizing it in this chapter for the optimum control current.

5.3   Optimum Design Procedure of Control Current

Figure 5.2 (a) shows a procedure for optimum design method of a control current I_g. First, the boundary condition, $I_{g,min}$ and $I_{g,max}$, of the control current is set from simulation results of frequency analysis for each I_g. For modeling a distortion of the filter, DC simulations are performed for $I_{g,min} \leq I_g \leq I_{g,max}$ and then coefficients α_i $(i = 0, 1, 2, \ldots)$ and β_2 in Eqs. (5.5) and (5.6) are obtained from the LSM. Next, an equivalent input noise voltage PSD $\overline{v_{nf1}^2}$ is measured by noise simulation. Finally, an optimum control current $I_g(I_i)$ can be numerically given by finding a locus through peak SNDRs in Eq. (5.9) for each I_g.

A numerically method for obtaining an optimum control current is shown in Fig. 5.2 (b) where an appropriate boundary condition for I_i is also introduced as $I_{i,min} \leq I_i \leq I_{i,max}$. In Fig. 5.2 (b) peak SNDRs are searched for each I_i from an initial condition $(I_{i,min}, I_{g,min})$ to $(I_{i,max}, I_{g,max})$. Note that it is assumed that an optimum $I_g(I_i)$ becomes a monotone function between $(I_{i,min}, I_{g,min})$ and $(I_{i,max}, I_{g,max})$. It would be said that this assumption is valid from an experience in Ref. [26].
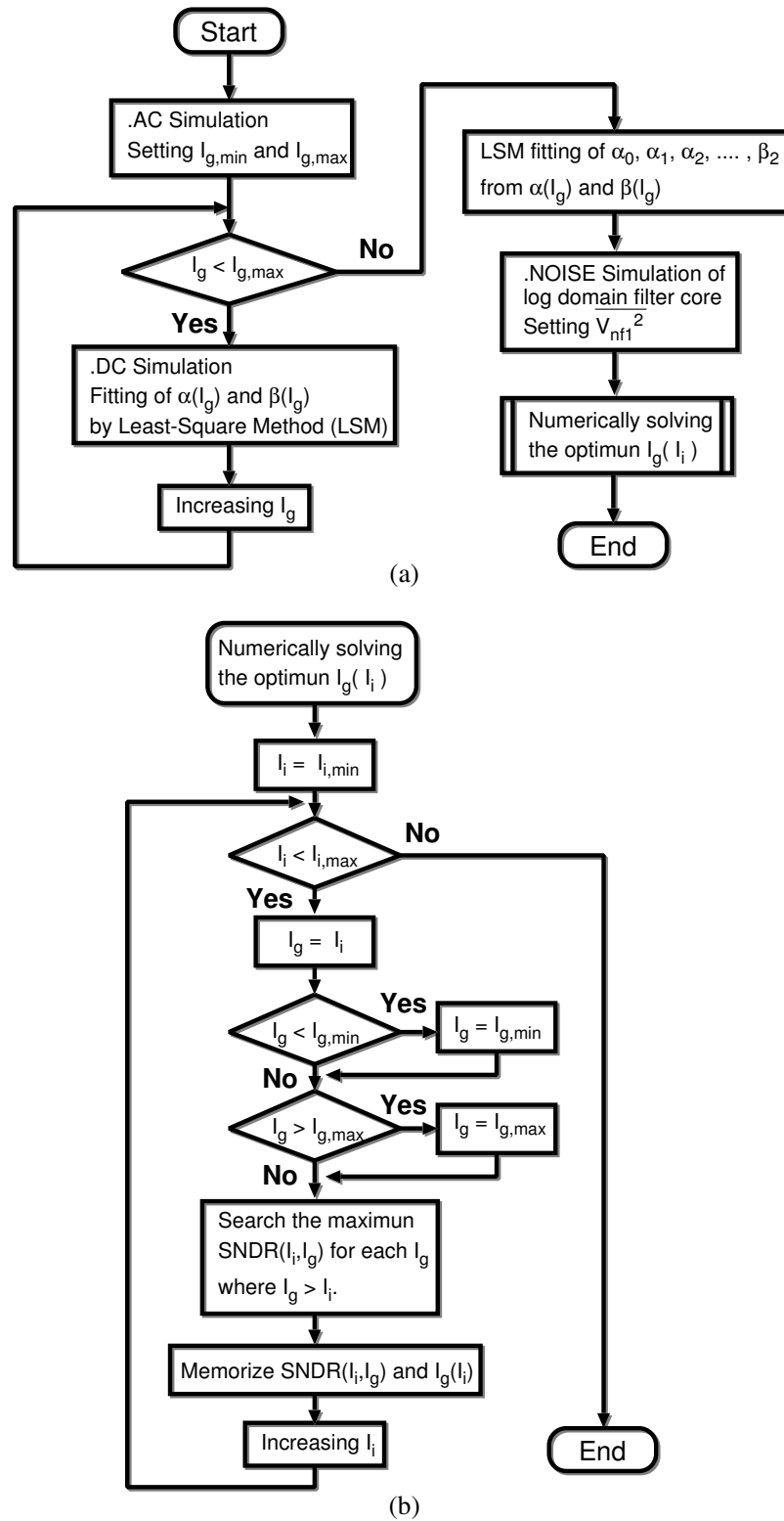
Figure 5.2: (a) Procedure for an optimum control current design and (b) numerically method for finding a locus of an optimum control current.
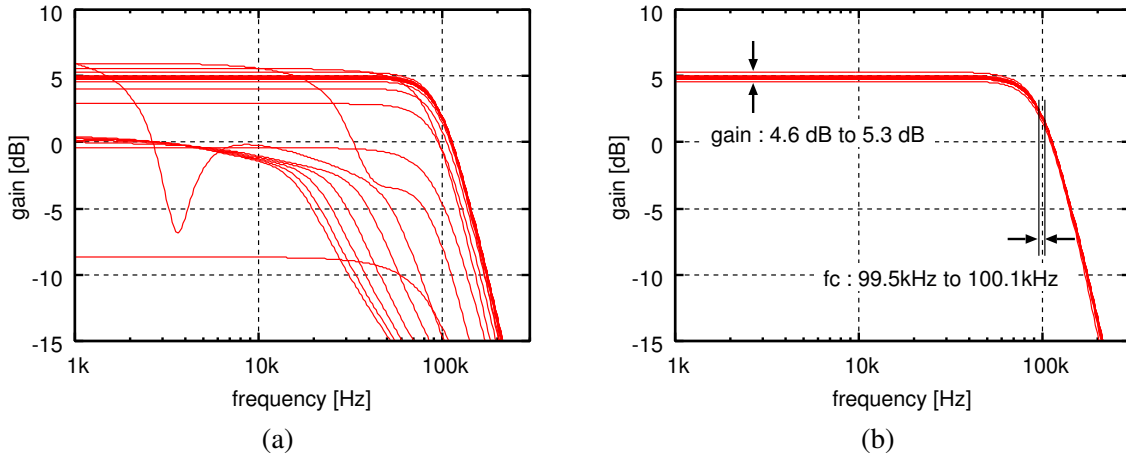
Figure 5.3: Frequency responses for each I_g. (a) I_g is 1 nA to 1 mA and (b) I_g : 30 nA to 300 μA

Although the proposed method shown in Fig. 5.2 needs some simulations which are AC, DC, and noise, the total simulation time is less than obtaining SNDR from transient simulations for all combinations of I_g and I_i. Therefore the proposed method is effective to expect an optimum control current in a short time.

5.4 Design Example

This section describes a design example of a control current to verify effectiveness of the proposed method shown in Fig. 5.2. The designed optimum control current $I_{g,prop}$ from Fig. 5.2 is compared to a control current $I_{g,sim}$ from transient simulations for all combination of I_g and I_i. A 3$^{\text{rd}}$-order Butterworth low-pass filter with a 100-kHz cutoff frequency is assumed here. In this case an equivalent noise bandwidth f_{NBW} in Eq. (5.9) becomes 300 kHz. From the procedure in Fig. 5.2 (a), first, frequency responses of the filter are obtained by SPICE simulations and shown in Fig. 5.3 (a) where I_g is from 1 nA to 1 mA. If it is assumed that available variations of the frequency response for change of I_g are a cutoff frequency of a $\pm$1-% variation and a passband gain one below 1 dB, then a boundary condition of I_g becomes

$$I_{g,min} = 30\text{nA} \leq I_g \leq 300\mu\text{A} = I_{g,max} \tag{5.13}$$
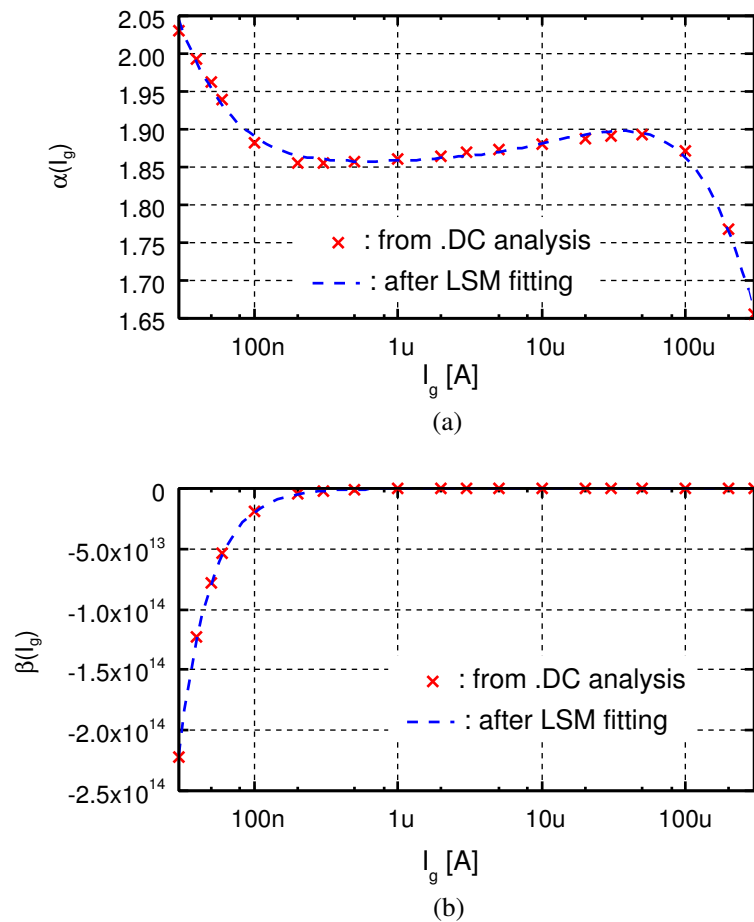
Figure 5.4: Coefficients α and β for each $I_g(I_i)$.

and thus, frequency response is redrawn as in Fig. 5.3 (b) under the range. Next, coefficients α and β in Eqs. (5.5) and (5.6) are obtained from DC simulations for each I_g and plotted as in Fig. 5.4 (a) and (b), respectively. In this figure, the marks 'x' imply results of DC simulation and the dashed lanes are from Eqs. (5.5) and (5.6) after LSM fitting where order in Eq. (5.5) is until $i = 5$ and their coefficients are listed in Table 5.1. Furthermore a coefficient $\beta_2 = -0.198$ in Eq. (5.6) is also obtained by LSM fitting. An input-referred equivalent noise voltage PSD of a stand-alone log domain filter core is shown in Fig. 5.5. From the result in the passband, $\overline{v_{nf1}^2} = 2.15 \times 10^{-15}$ V^2/Hz is found.

Figure 5.6 shows SNDR for I_i and I_g, which is obtained by transient simulation results for all combination of I_g and I_i. In this case the total simulation time is about

Table 5.1: Coefficients in Eq. (5.5).

α_0	-48.6889
α_1	-19.8353
α_2	-3.08972
α_3	-0.239295
α_4	-0.00922813
α_5	-0.000141906
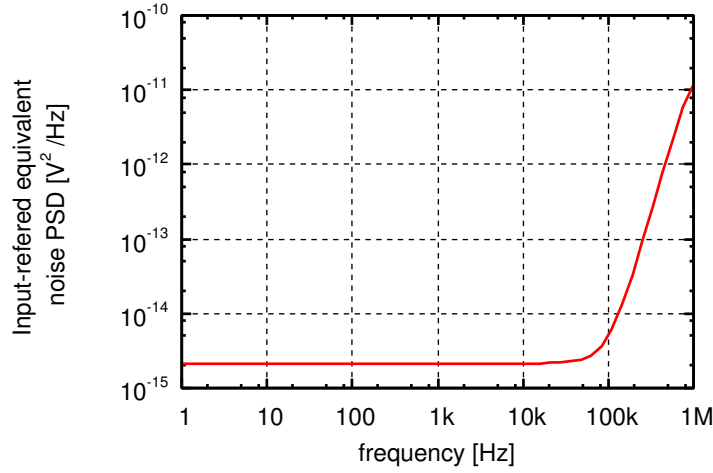
Figure 5.5: Input-referred equivalent noise voltage PSD of a log domain filter core.

four hours. On the other hand, using Eq. (5.9) and Fig. 5.2 (b), an analytical optimum control current $I_{g,prop}$ shown in Fig. 5.7 is obtained under a boundary condition of $(I_i, I_g) = (10 \text{ pA}, 30 \text{ nA})$ to $(0.5 \text{ mA}, 300 \text{ } \mu\text{A})$, where the optimum control current $I_{g,sim}$ from Fig. 5.6 is also shown in the same figure. As seen from the results, $I_{g,prop}$ meets the true optimum control current $I_{g,sim}$ from transient simulation results. The total simulation time of the proposed method including frequency response, DC, and noise simulation is less than five minutes. Furthermore Fig. 5.8 shows SNDRs of the filter, which are calculated by using each control current, $I_{g,prop}$ and $I_{g,sim}$, in Fig. 5.7. From the figure it is confirmed that the filter can approximately be designed to achieve an optimum SNDR in a short time.
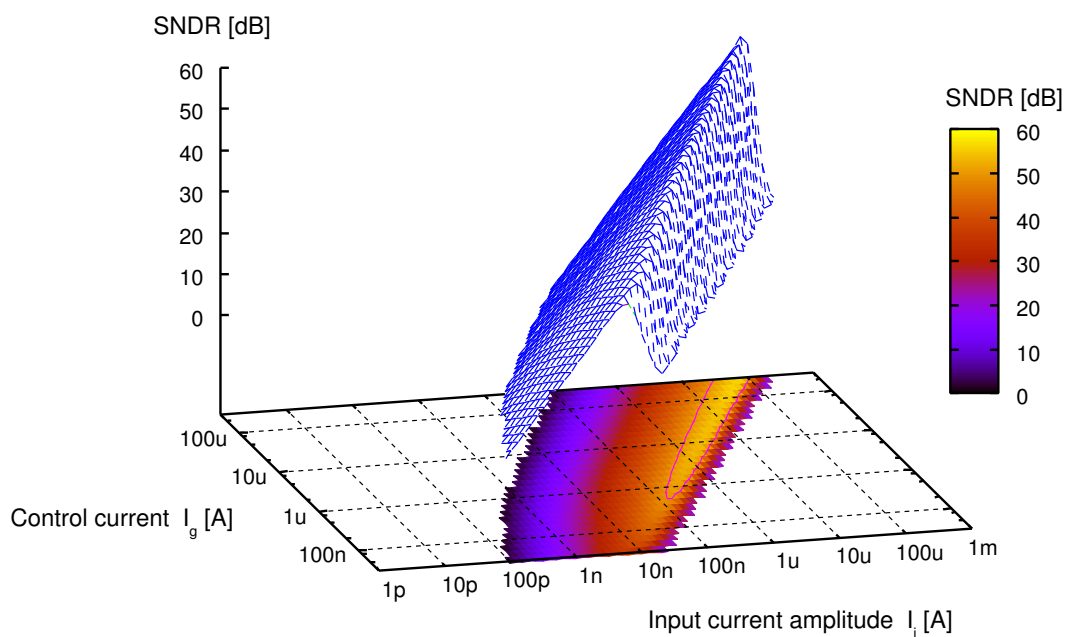
Figure 5.6: SNDR from transient-based simulation results.
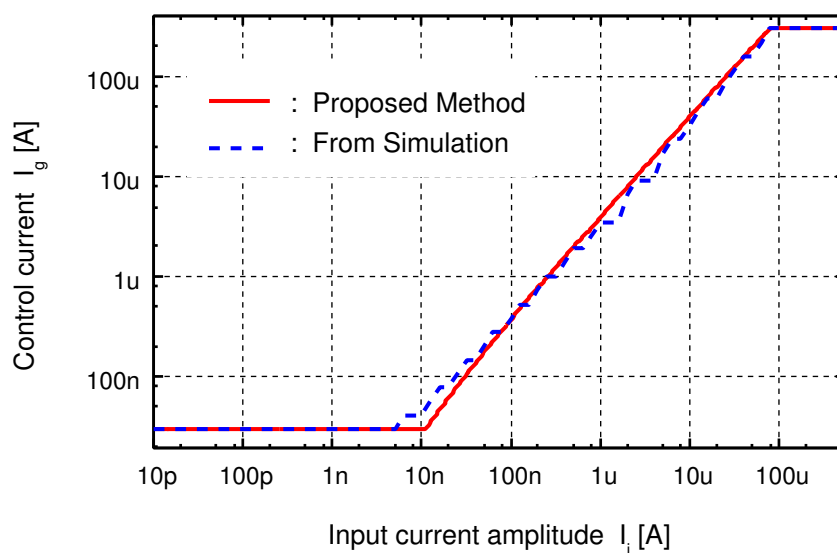
Figure 5.7: Analytical optimum control current by proposed method and practical optimum control current based on transient simulations.
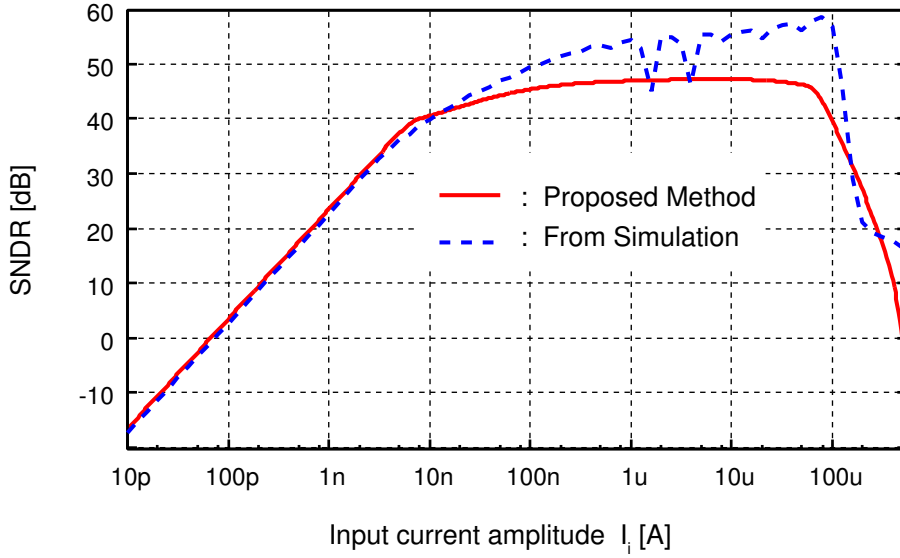
Figure 5.8: SNDRs of the filter by using each control current in Fig. 5.7.

5.5   Discussion for control current generation

The best SNDR curve of the filter is provided by the proposed method as described in the previous sections, which is obtained by use of an ideal envelope detector. In this case the control current and the SNDR curve are shown in Fig. 5.9 (a). In a practical filter design, a filter in an application requires an SNDR which is greater than a specified SNDR, $\text{SNDR}_{\text{spec.}}$. An input range for $\text{SNDR} \geq \text{SNDR}_{\text{spec.}}$, or an output range, is called as usable dynamic range (UDR). Therefore, a filter must be designed to satisfy a specified UDR for $\text{SNDR}_{\text{spec.}}$ [23]. In the viewpoint of implementation, it is difficult to design an ideal envelope detector for syllabic companding log domain filters because an output of the detector has a slight ripple as well to induce an output distortion of the filters. One solution for a ripple is to use quantized values of an input envelope. Recalling that a design of I_g has degree of freedom and a filter must satisfy a specified UDR for $\text{SNDR}_{\text{spec.}}$, then one can also use a discrete control current instead of an optimum one as shown in Fig. 5.9 (b). In this figure a control current I_g takes four values with greater than $\text{SNDR}_{\text{spec.}}$ over the UDR. More details of circuit implementations will be described in Chapter 6.
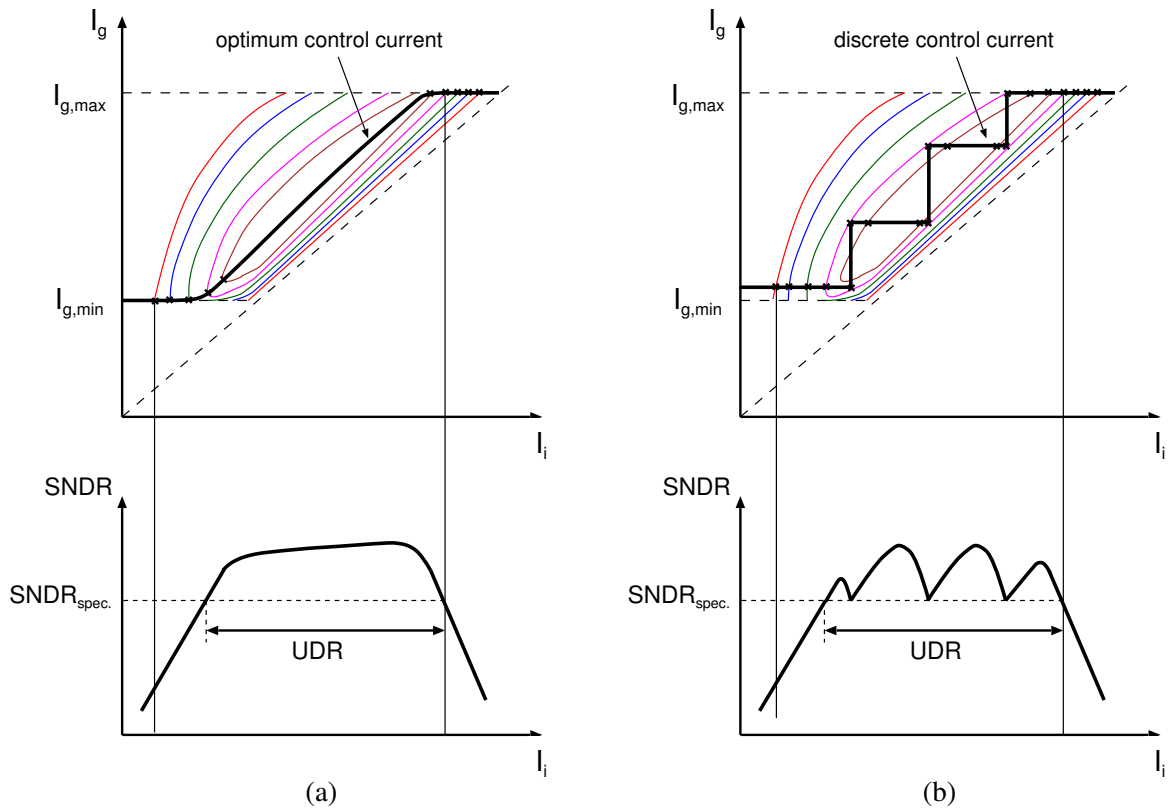
Figure 5.9: SNDRs at different locus of control current: (a) optimum and (b) discrete.

5.6 Conclusion

This chapter proposes a design method of an optimum control current for large SNDR. Since the method needs only short-time simulations, that are DC, AC, and noise analysis, significant suppression of the design time is brought in comparison with a method using transient simulations. A design example is described for verification of the proposed method and then its effectiveness is confirmed: a simulation time is reduced by a factor of about (5 minutes)/(240 minutes) = 1/48. Furthermore the control current generation is discussed in terms of a practical implementation and a specified SNDR.

Chapter 6

Low-Voltage Biasing Circuits and Automatic Frequency Tuning System for Syllabic Companding Log Domain Filters

6.1   Introduction

The proposed low-voltage syllabic companding filters require several biasing circuits. A peak detector, which senses a peak of an input or an output current of the filters, is used to generate a control current according to a manner as described in Chapter 5. Furthermore a voltage reference circuit to enhance tolerance for variation of temperature or supply voltage and a frequency tuning system which adjusts a cutoff frequency of the filter to a desired value, are needed in the filters. These biasing circuits for syllabic companding log domain filters must be designed at a low-power supply of 0.8 V in 0.35-μm CMOS and 0.6 V in 0.18-μm one.

In this chapter these low-voltage biasing circuits are designed. First a low-voltage current peak detector as a control current generator is proposed using an equivalent diode circuit and is fabricated in a 0.35-μm CMOS process. Another approach is also described by quantizing the peak of the signals. Next a voltage reference circuit is designed by replacing bipolar transistors of a conventional bandgap reference circuit with MOSFETs in weak inversion region. Finally a frequency tuning system is proposed for log domain filters and its stability is considered. The system employs a charge pump circuit instead of an amplifier with high gain for low-voltage operation.

6.2　Control Current Generator

6.2.1　Low-Voltage Current Peak Detector

Proposed Low-Voltage Configuration Figure 6.1 (a) shows a voltage-mode peak detector composed of a diode D_1, an operational amplifier A_1, a holding capacitor C_H, and a discharge resistor R_D. If an output voltage V_{out} is less than V_{in}, the A_1 outputs high level and then C_H is charged through D_1 to follow the peak voltage of the V_{in}. The R_D makes it possible for V_{out} to follow the peak of the decreasing V_{in}. The peak-detection range is limited by the common-mode input range of the amplifier A_1 under low-supply voltage.

A current-input and output realization of the voltage-mode peak detector shown in Fig. 6.1 (a) is illustrated in (b) and its CMOS implementation done in (c). The block A_2 in Fig. 6.1 (b) operates as a current comparator which compares an input current I_{in} with an output current I_{out}. In Fig. 6.1 (c) the comparator A_2 is realized by MOSFET M_{in} and its drain resistor. In Refs. [77] and [78] a diode-connected n-channel MOSFET is used as a diode in Fig. 6.1 (c). In this case, however, a potential of the drain terminal of M_{in} is relatively high because of added gate-to-source voltage of the diode-connected MOSFET between gate and drain terminal of M_{in}.

Figure 6.1 (d) shows a proposed equivalent diode circuit in which all MOSFETs are biased in weak inversion region [79]. In this circuit, Kirchhoff's voltage law (KVL) gives $V_i - nU_T \ln(I_{d1}/I_S) = V_o - nU_T \ln(I_B/I_S)$ and thus its output current I_{d1} can be expressed as

$$I_{d1} = I_B \exp\left(\frac{V_i - V_o}{nU_T}\right) \tag{6.1}$$

where I_B is a bias current, and n and U_T are a slope factor and a thermal voltage, respectively. Equation (6.1) means that the proposed circuit is an equivalent diode circuit. This equivalent diode circuit has two advantages compared to a diode-connected MOSFET. One is that no drop voltage is needed between V_i and V_o. Another is that the current comparator M_{in} of Fig. 6.1 (c) does not need to drive D_1 with a large
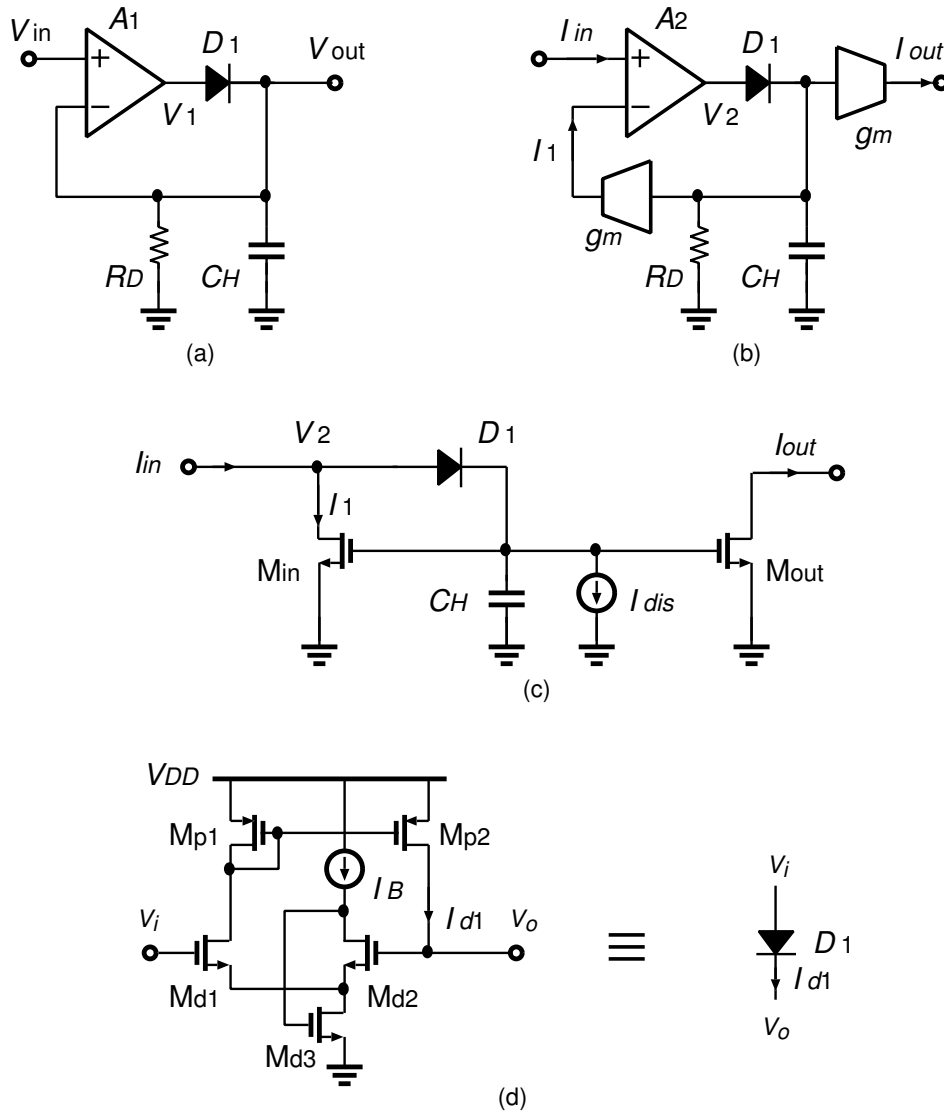
Figure 6.1: Peak detector. (a) Voltage-mode approach. (b) Current-mode approach. (c) CMOS implementation of (b). (d) Low-voltage equivalent diode with a zero drop voltage between V_i and V_o.

output current because an input impedance of this circuit is very high. Therefore, use of this equivalent diode circuit is suitable for low-voltage operation.

Measured Results   A prototype chip of the current peak detector using the proposed equivalent diode circuit is fabricated in a 0.35-μm standard CMOS process. The total area is about 450 μm $\times$ 680 μm. A micrograph of the current peak
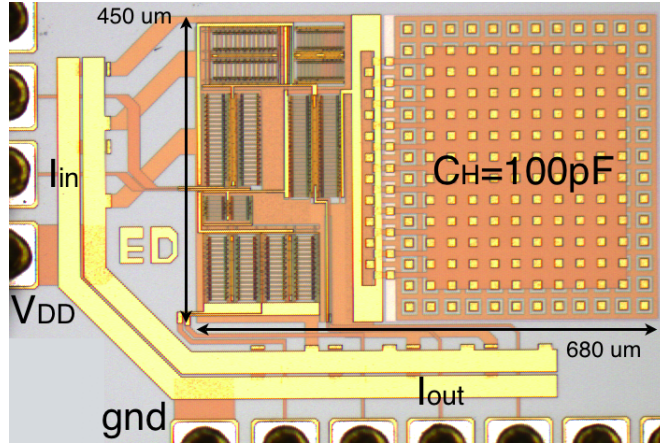
Figure 6.2: Microphotograph of the proposed peak detector.

detector in Fig. 6.1 (c) including the equivalent diode circuit in (d) and a 100-pF holding capacitor C_H is shown in Fig. 6.2. In the measurements, an input current is applied from a voltage of a function generator through an external 100-kΩ resistor and an output current is sensed through an external operational amplifier and 100-kΩ resistor. The following measurement is taken at a power supply of 0.8 V.

Figure 6.3 (a) shows transient output waveforms for 100-kHz sinusoidal input currents I_{in} with different input current amplitudes where a discharge current I_{dis} and a bias current I_B used in Fig. 6.1 equal to 230 nA and 10 μA, respectively. A behavior of a change of discharge time constant with I_{dis} varied is shown in Fig. 6.3 (b). The larger I_{dis} becomes, the faster the discharge time of C_H. The discharge time constant of the peak detector is varied depending on the input current amplitude because of constant I_{dis} as seen from Fig. 6.3 (a). If a signal independent discharge time constant is needed, βI_{out} can be applied as the discharge current instead of a constant I_{dis} where β is a constant coefficient and obtains a signal independent discharge time constant [78].

Figure 6.4 shows the input current amplitude versus the peak value of the output current. The measured plot approximately agrees with the simulated one. It is confirmed that wide-detection range is achieved under low-supply voltage.
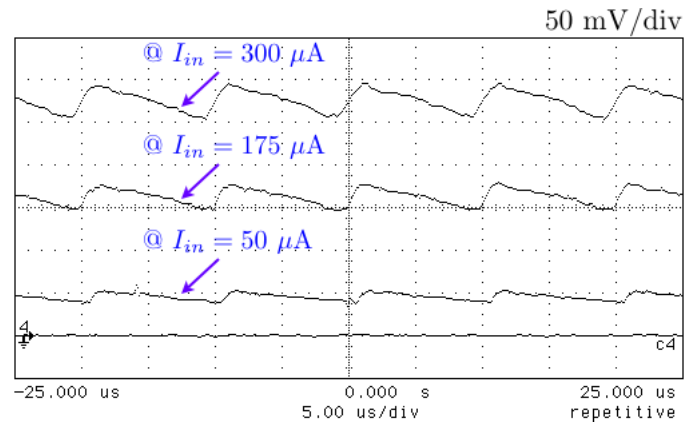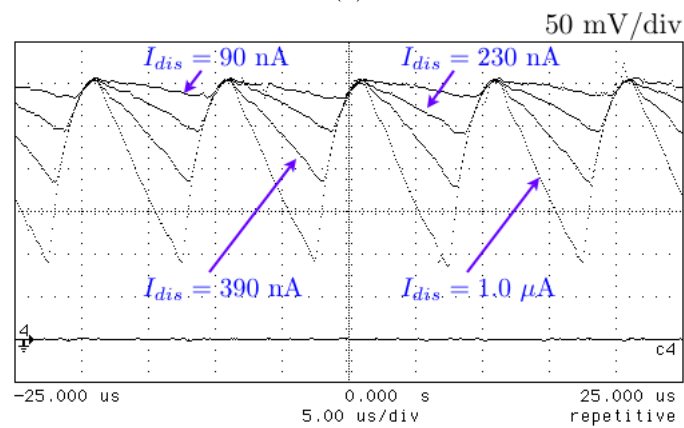
Figure 6.3: The measured output current waveforms of the peak detector at a 100-kHz sinusoidal input current. (a) The waveforms for different input current amplitude and (b) discharge current I_{dis}.
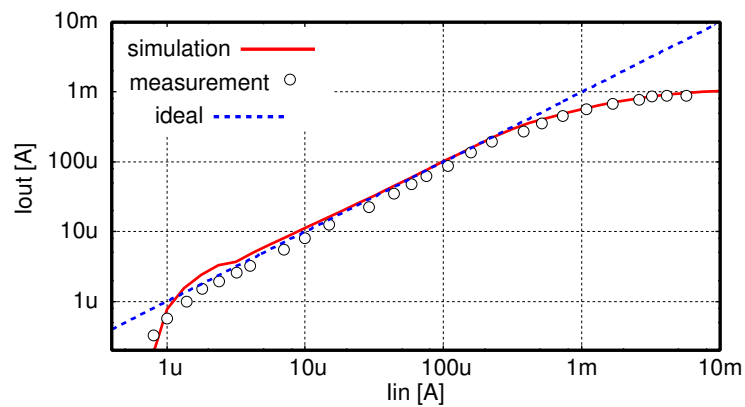
Figure 6.4: Input current amplitude v.s. peak value of output current.

6.2.2 Piece-wise Constant Current Generator

Another approach to generate a control current I_g is to quantize a peak of an input or an output current of the filters instead of the current peak detector shown in Fig. 6.1 (c) the output of which inherently has a ripple as shown in Fig. 6.3. The ripple influences an output current of the filters as a distortion due to non-ideality of MOSFETs [68]. If the peak is quantized at a regular interval, an output as the control current I_g is free of the ripple except for a change of its value.

Figure 6.5 (a) shows a three-value quantized peak detector [68]. In Fig. 6.5 (a), the comparator A_1, diode D_1, and a holding capacitor C_H compose a voltage peak detector of V_1 which is converted from I_{inp} by the diode-connected MOSFET M_a. The output of A_1 becomes high only when V_1 is greater than a hold voltage V_2, and then the C_H is charged by a current flowing through the diode D_1 to make V_2 hold a peak value of V_1. In order to discharge a charge of C_H, an inverter, a switch, and M_d are added. M_d produces a discharge current I_{dis} which decides discharge speed of C_H. Two comparators A_2 and A_3 compare the peak voltage V_2 with two reference voltages, which are determined by reference currents I_{ref1} and I_{ref2} through diode-connected MOSFETs M_b and M_c. Then, two 1-bit signals of comparison results are fed to a decoder for switching reference current sources through D Flip-Flops (DFFs). Although the outputs of A_2 and A_3 probably very often flop due to ripple of V_2, frequent switching is undesirable. For relaxing this issue, DFFs load outputs of the comparators only when the output of A_1 is high, i.e. in a charge phase for C_H. Any of the decoded three signals is high and a corresponding current, I_{ref1}, I_{ref2}, or I_{ref3}, is selected as a quantized peak current of I_{inp}. This current flows into M_{p5} and M_{p6} mirrors it. A resistor R_L and a capacitor C_L are employed as a simple low-pass filter for avoiding a rapid change of the control current I_g, which leads to an error of a state variable correction. A schematic of comparators A_1, A_2, and A_3 used here is shown in Fig. 6.5 (b) where a positive feedback (regenerative) configuration is employed for fast switching. Furthermore the diode D_1 in Fig. 6.5 (a) is realized by the equivalent circuit shown in Fig. 6.5 (c) the configuration of which is the same as
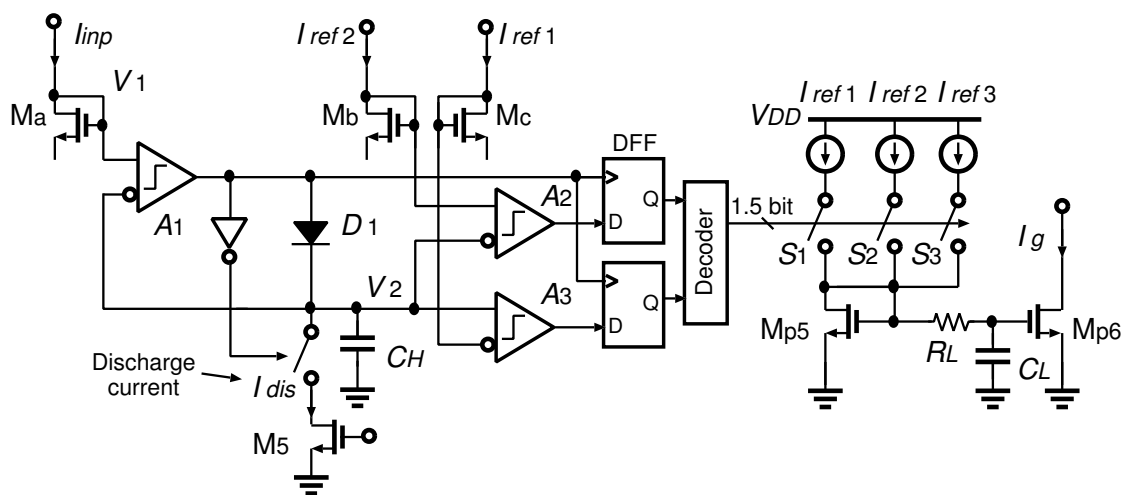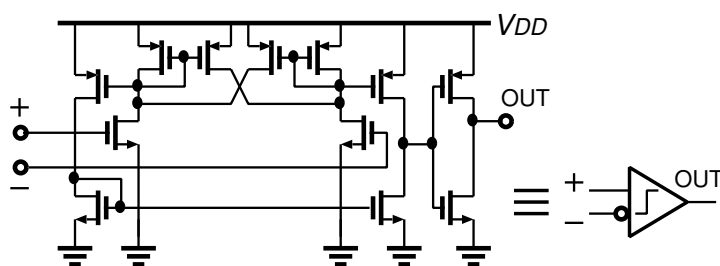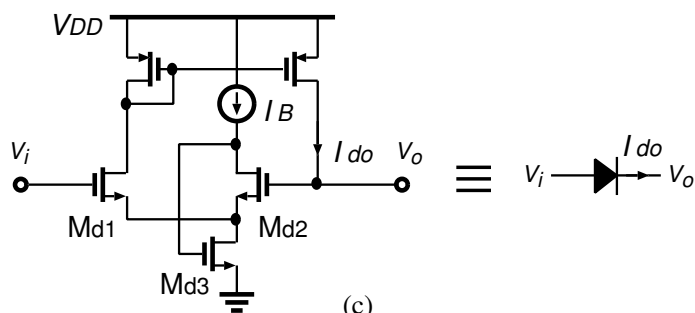
Figure 6.5: Piece-wide constant control current generator: (a) three-value quantized peak detector, (b) comparator circuit A_1, A_2 and A_3, (c) equivalent diode circuit with a high-input impedance, and diagram for the switches.
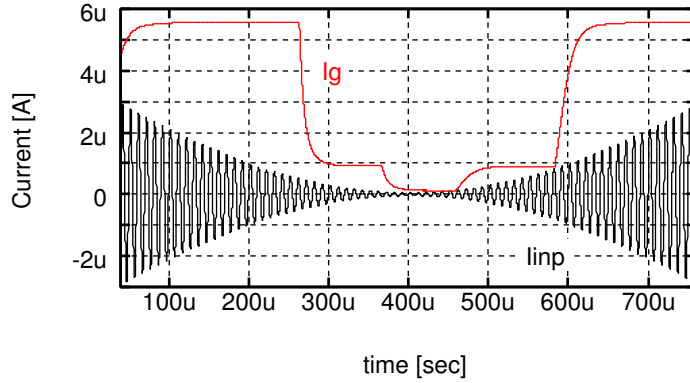
Figure 6.6: A response of the control current I_g for the input current I_{inp} with envelope sweep.

that in Fig. 6.1(d). A relation between the input current I_{inp}, state of the switches, and the control current I_g is summarized in Fig. 6.5 (d).

Figure 6.6 shows a response of the control current I_g when the envelope of the input current I_{inp} changes. In the simulation the reference currents I_{ref1}, I_{ref2}, and I_{ref3} are set as 100 nA, 900 nA, and 5.6 μA, respectively. As seen from the result it is confirmed that the control current I_g has no ripple.

The piece-wide constant current generator in Fig. 6.5 (a) employs a resistor R_L and a capacitor C_L in order to relax a rapid change of I_g. Nevertheless a fast edge remains at a certain extent as seen from Fig. 6.6 at a moment of change of I_g, which makes an output of the filter distort because of a non-ideality of a state variable correction circuit. For more relaxing the fast edge, a circuit shown in Fig. 6.7 (a) is available, which utilizes an external clock, several current sources, and DFFs. In Fig. 6.7 (a) if a signal labeled as "I_g control" goes up, then the current sources except for the rightmost one, I_{ref1}, turn on and a total current I_a becomes I_{ref2} synchronizing with the clock as shown in Fig. 6.7 (b) where each current source with switches has different weight as shown in Fig. 6.7 (a). Therefore the fast edge change of the control current I_g can be eliminated by applying the appropriate weight to the current sources.
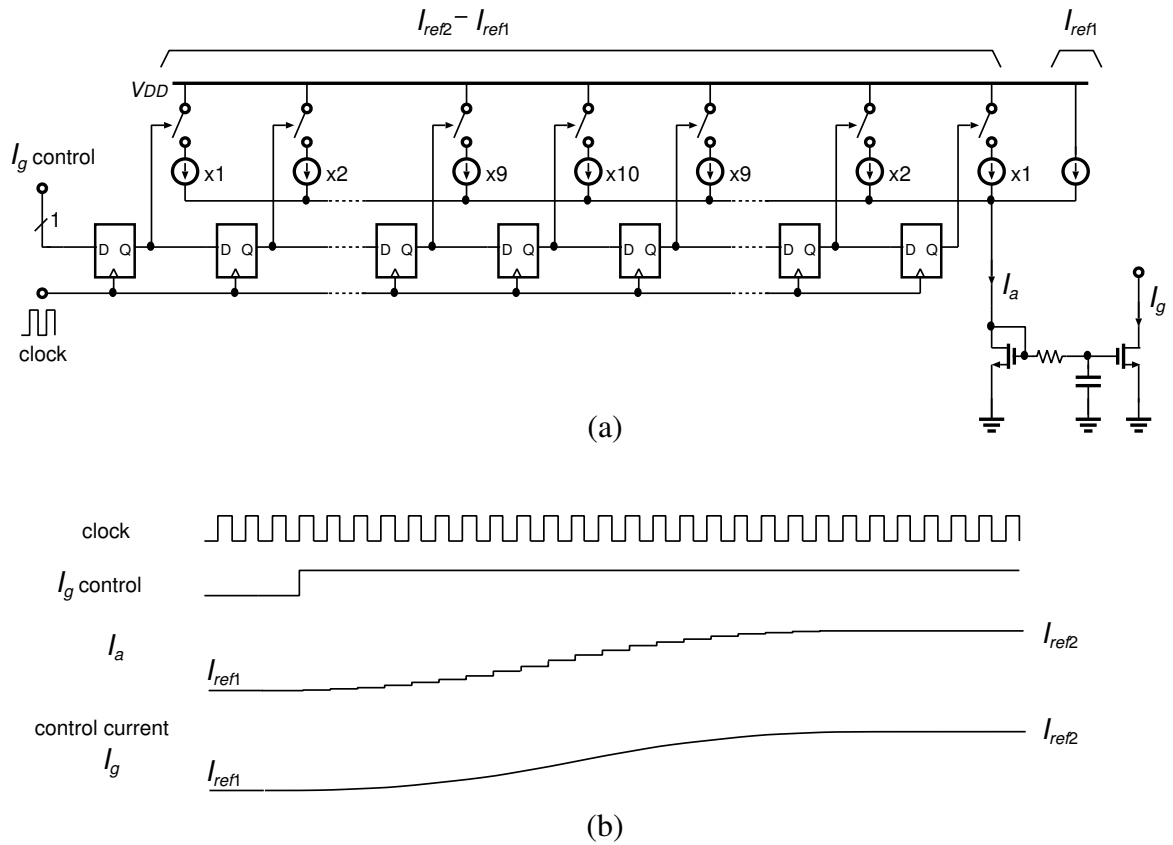
Figure 6.7: An output stage of the control current generator for smooth change of I_g. (a) the circuitry and (b) its timing diagram.

6.3   Voltage Reference Circuit under Low-Supply Voltage

The proposed syllabic-companding log domain filters require a voltage reference circuit which must be insensitive for variation of temperature and supply voltage. Furthermore the reference circuit must output a voltage of 0.4 V for V_b in Figs. 4.3 or 4.5 from a power supply of 0.6 V.

Figure 6.8 shows a low-voltage reference circuit which is the same configuration as a conventional bandgap reference circuit [80] except for using p-channel MOSFETs M_1 to M_3 as a parasitic diode. Although a parasitic diode is generally employed in a bandgap reference circuit for obtaining a temperature coefficient in a bandgap energy of pn junction, the drop voltage of the diode becomes about 0.7 V, which makes low-voltage operation of a bandgap reference circuit difficult. On the other hand, since
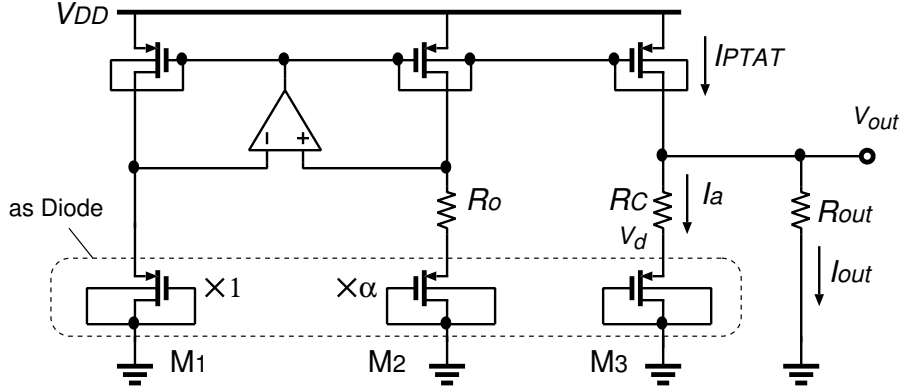
Figure 6.8: Low-voltage reference circuit.

the designed voltage reference circuit shown in Fig. 6.8 uses p-channel MOSFETs in weak inversion region, its drop voltages become less than 0.4 V and a temperature coefficient is obtained as in the case of using diode. In the figure, Kirchhoff's voltage law (KVL) at a non-inverting terminal of an operational amplifier gives

$$nU_T \ln \frac{I_{PTAT}}{I_s} = nU_T \ln \frac{I_{PTAT}}{\alpha I_s} + I_{PTAT}R_0 \tag{6.2}$$

and thus a current I_{PTAT} is expressed as

$$I_{PTAT} = \frac{n \ln \alpha}{R_o}U_T. \tag{6.3}$$

Since a thermal voltage U_T is proportional to absolute temperature: $U_T = kT/q$, a current I_{PTAT} in Eq. (6.3) is so, too. On the other hand, an output voltage V_{out} becomes

$$V_{out} = R_{out}I_{out} \tag{6.4}$$

and then if one subtracts I_{PTAT} from a current I_a which is proportional to absolute temperature, I_{out} or V_{out} becomes independent for variation of temperature. If an arbitrary R_{out} for a desired V_{out} is provided, a current I_a is expressed as

$$I_a = I_{PTAT} - I_{out} = \frac{n \ln \alpha}{R_o}U_T - \frac{V_{out}}{R_{out}} \tag{6.5}$$

and solving for V_{out},

$$V_{out} = nU_T \ln \alpha \frac{R_{out}}{R_o} - I_aR_{out} \tag{6.6}$$

is obtained. Since V_{out} must be independent for temperature: $\partial V_{out}/\partial T = 0$, the above equation is transformed into

$$\frac{\partial I_a}{\partial T} = \frac{n}{R_o} \ln \alpha \frac{\partial U_T}{\partial T}. \tag{6.7}$$

On the other hand, from relations of $V_{out} = R_C I_a + V_d$ and $\partial V_{out}/\partial T = 0$,

$$\frac{\partial I_a}{\partial T} = -\frac{1}{R_C} \frac{\partial V_d}{\partial T} \tag{6.8}$$

are given. Therefore, since Eqs. (6.7) and (6.8) are equal, R_C is uniquely provided as

$$R_C = -\frac{R_o}{n \ln \alpha} \left(\frac{\partial U_T}{\partial T} \right)^{-1} \frac{\partial V_d}{\partial T}. \tag{6.9}$$

Note that $\partial V_d/\partial T$ is a coefficient which is measured under a constant current for MOSFETs as a diode; for instance -0.98 mV/K at 1.0-μA and $T = 0$ K. As a result, using the resistance determined from Eq. (6.9), the output reference voltage is expressed as

$$V_{out} = \left(1 + \frac{R_{out}}{R_C} \right)^{-1} \cdot \left(n U_T \frac{R_{out}}{R_o} \ln \alpha + \frac{R_{out}}{R_C} V_d \right). \tag{6.10}$$

In Eq. (6.10) assuming that all temperature coefficients of resistors have the same value and a drop voltage V_d is determined at a desired temperature, then the output voltage V_{out} is insensitive for variation of temperature.

The voltage reference circuit shown in Fig. 6.8 is designed using a 0.18-μm CMOS process and simulated where a supply voltage V_{DD} is 0.6 V. In Fig. 6.8 the design parameters are set as shown in Table 6.1 for generating an output voltage V_{out} of 0.4 V. Figure 6.9 (a) shows output voltages for supply voltage V_{DD} at each temperature and (b) is its expanded figure around $V_{DD} = 0.6$ V. In the figure it is confirmed that the designed circuit outputs a desired voltage, 0.4 V, from $V_{DD} = 0.55$ V and has no dependency for variation of temperature. Figure 6.10 (a) shows an output voltage V_{out} and (b) does its fractional temperature coefficient TC for temperature variation. The coefficient TC is defined as a following equation [30]:

$$TC = \frac{1}{V_{out}} \frac{\partial V_{out}}{\partial T} \tag{6.11}$$

Table 6.1: Design parameters for voltage reference circuit.

R_o	16.23 kΩ
R_C	54.1 k Ω
R_{out}	140.66 kΩ
α	8
$M_1 : W/L$	19.2 μm / 0.9 μm
$M_2 : W/L$	$\alpha \times$ 19.2 μm / 0.9 μm
$M_3 : W/L$	$4 \times$ 19.2 μm / 0.9 μm
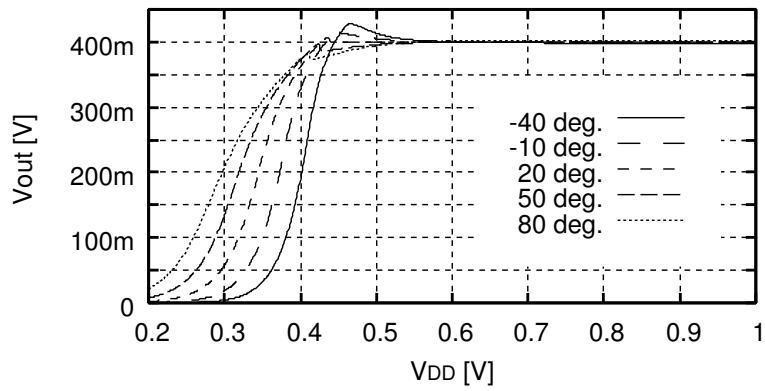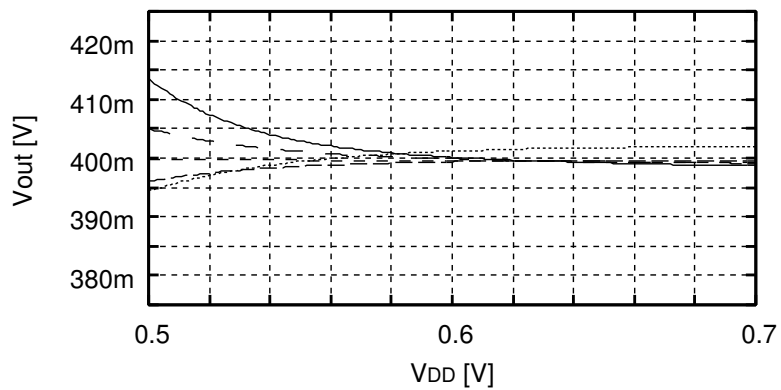
Figure 6.9: Output voltage versus supply voltage for each temperature.
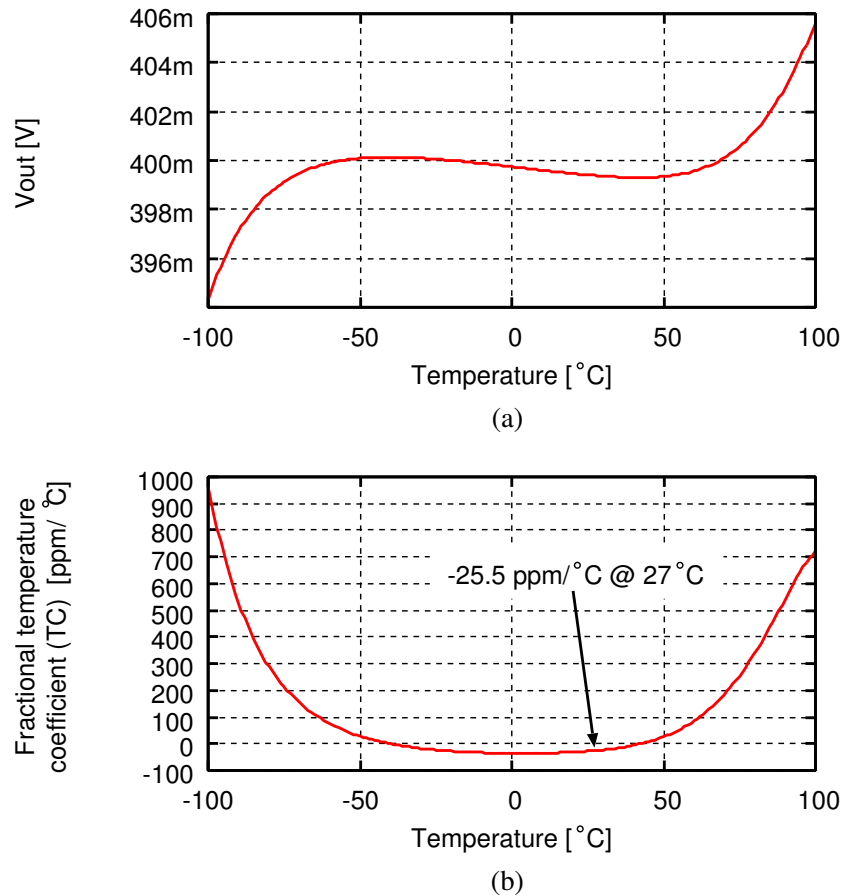
Figure 6.10: Temperature variation: (a) output voltage and (b) temperature coefficient (TC).

and at a room temperature 27 °C the coefficient is $TC = -25.5$ ppm/°C. For the range from -100 °C to 100 °C, although the output voltage varies about ± 5 mV, this variation does not very affect to the proposed syllabic companding log domain filters.

The voltage reference circuit is fabricated in a 0.18-μm CMOS process and measured at room temperature. The chip microphotograph is shown in Fig. 6.11 and the circuit occupies an area of 350 μm $\times$ 480 μm. Figure 6.12 shows measured supply-voltage dependency and its expanded figure. Although the measured voltage is 2 mV larger then the simulated one, it is confirmed that the circuit is insensitive for a variation of supply voltage at a room temperature.
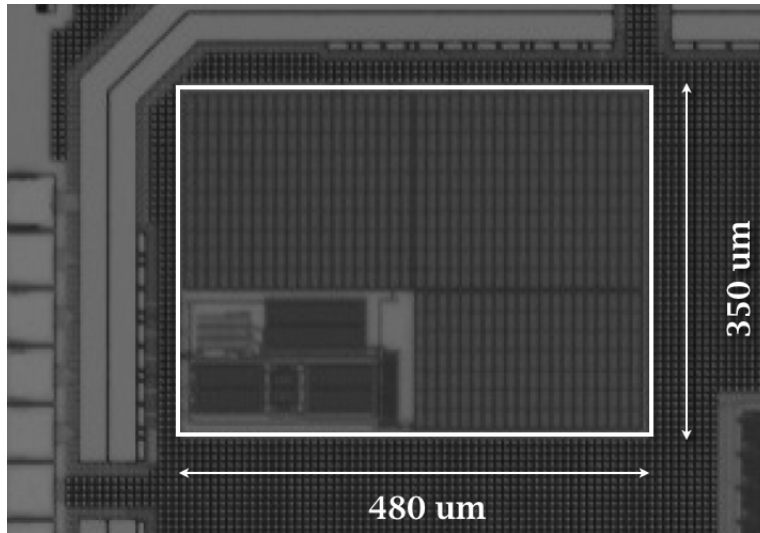
Figure 6.11: Chip microphotograph of the voltage reference circuit.
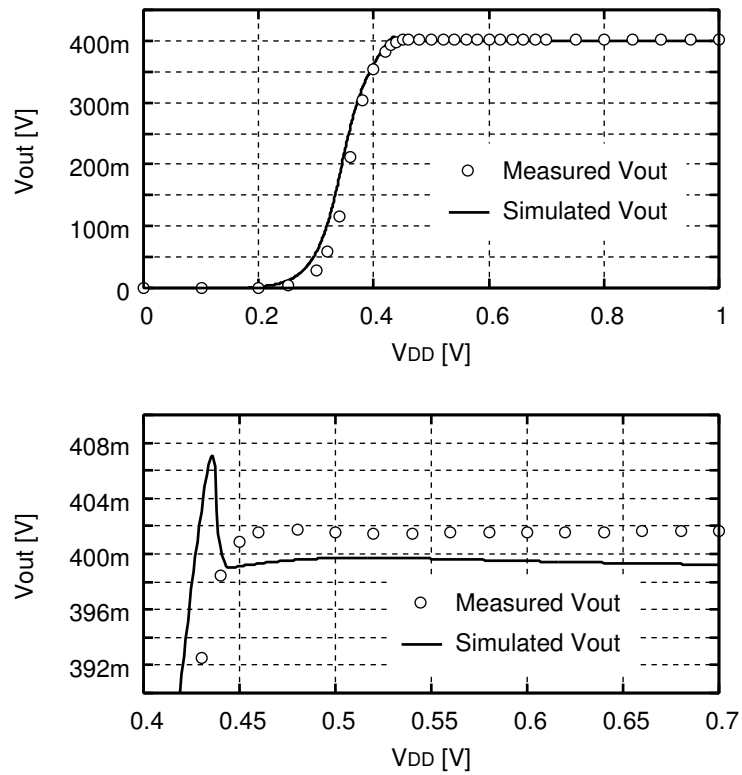
Figure 6.12: Measured result of the voltage reference circuit under room temperature.
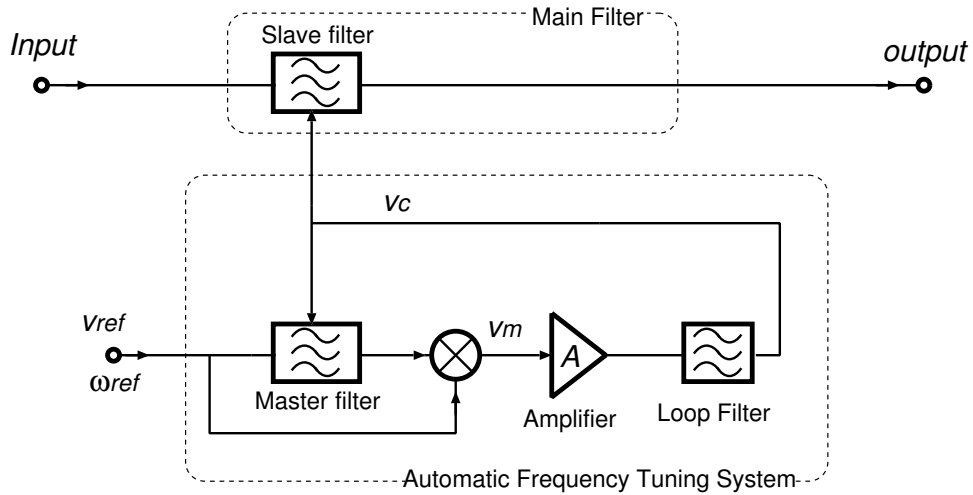
Figure 6.13: A frequency tuning system based on voltage-controlled filter (VCF).

6.4 Frequency Tuning System for Log Domain Filter

6.4.1 Proposed Architecture based on Voltage Controlled filter

The cutoff frequency of a filter based on integrators is automatically adjusted by using several tuning systems proposed in Refs. [81]–[83]. In general all of the systems controls a voltage V_C, which is proportional to a unity gain angular frequency Ω of integrators, to obtain a desired cutoff frequency by utilizing phase locked loop (PLL) strategy. In proposed syllabic companding log domain filters, its filter core is composed of log domain integrator cores and such tuning systems would also be applicable to the filter based on log domain integrators to adjust its cutoff frequency. However an issue exists to design the system under low-supply voltage. For the issue a new frequency tuning system is proposed in this section.

First, a principle of a tuning system is described. Figure 6.13 shows a filter with a conventional frequency tuning system based on voltage-controlled filter (VCF) technique, in which a master filter as a replica of a main filter is designed as a second-order low-pass filter using the same integrator with that of the main filter. Hence,

the transfer function of the master filter $H_{mst}(s)$ is expressed as

$$H_{mst}(s) = \frac{\Omega_c^2}{s^2 + \dfrac{\Omega_c}{Q}s + \Omega_c^2} \tag{6.12}$$

and the cutoff angular frequency Ω_c of the master filter is equal to that of the main filter. Since the cutoff frequency of the master filter is controlled by a negative feedback loop of the tuning system and then that of the main filter is also changed following to the master filter, the main filter is also called as a slave filter. Letting a reference signal V_{ref}, which is applied as an external signal, be a cosine wave with an amplitude of V_0 and an angular frequency of ω_{ref}, an output of the master filter becomes

$$|H_{mst}(j\omega_{ref})|V_0 \cos\{\omega_{ref}t + \arg H_{mst}(\omega_{ref})\} \tag{6.13}$$

and thus an output of a multiplier V_m is expressed as

$$\begin{aligned} V_m &= \frac{V_0^2|H_{mst}(j\omega_{ref})|}{2}[\cos\{\arg H_{mst}(j\omega_{ref})\} \\ &\qquad + \cos\{2\omega_{ref} + \arg H_{mst}(j\omega_{ref})\}]. \end{aligned} \tag{6.14}$$

For the signal V_m, multiplying a gain A of an amplifier and filtering a tone with $2\omega_{ref}$ by a loop filter, then a control voltage V_c is expressed as

$$V_c = \frac{A}{2}V_0^2|H_{mst}(j\omega_{ref})| \cdot \cos\{\arg H_{mst}(j\omega_{ref})\}. \tag{6.15}$$

Therefore V_c can be controlled by ω_{ref}. Furthermore, if the gain A is infinity, then $\cos\{\arg H_{mst}(j\omega_{ref})\} = 0$ and since $\arg H_{mst}(j\omega_{ref}) = -90°$, the cutoff frequency of the master filter almost becomes ω_{ref}. Therefore, the system shown in Fig. 6.14 also adjusts the cutoff frequency of the main filter as a slave one to ω_{ref}.

Low-supply voltage makes it difficult to design an amplifier with high gain in the VCF-based frequency tuning system shown in Fig. 6.14. For the issue a new method is proposed by use of a limiter, a charge pump (CP) circuit, and a duty ratio detector (DRD) instead of the amplifier. The CP can operate under low-power supply compared to an amplifier. Figure 6.14 shows a proposed VCF-based frequency
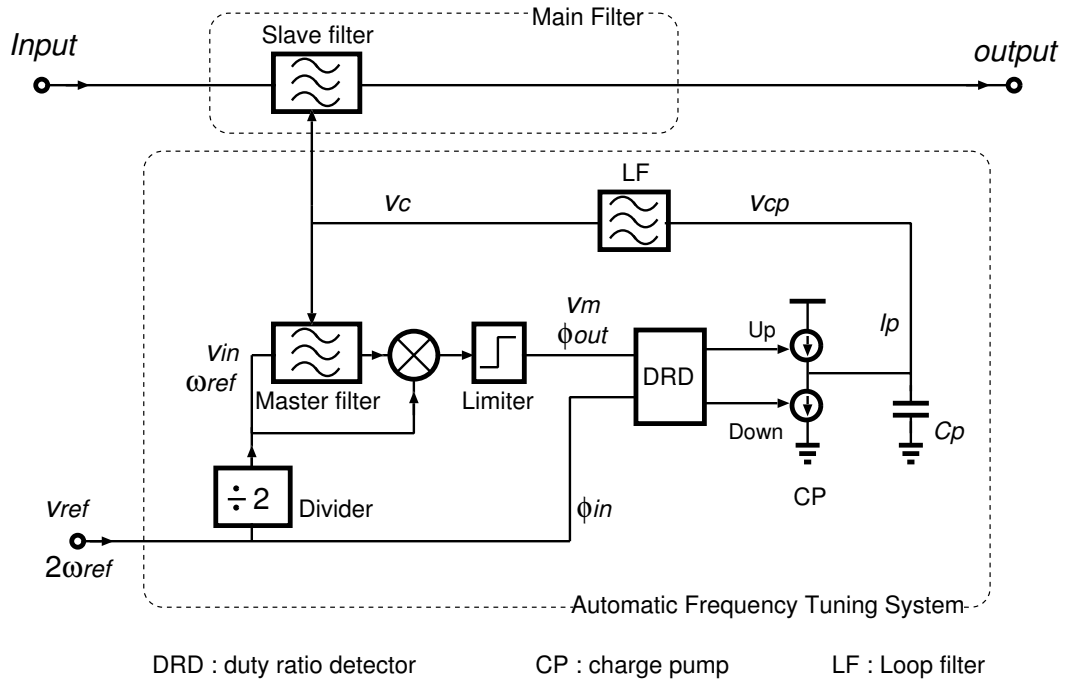
Figure 6.14: A block diagram of proposed VCF-based Frequency Tuning System.

tuning system. In the figure a reference clock V_{ref} with an angular frequency of $2\omega_{ref}$ is used, which is twice of a desired cutoff frequency. An output of a mixer is fed to a limiter and then a pulse V_m is obtained. If the slave and the master filters are log domain filters, the mixer is combined with the main filter as shown in Fig. 6.15. In Fig. 6.15 a reference signal V_{in} is converted to differential current pulse, I_{inp} and I_{inm}, by a direct digital synthesizer (DDS). The master filter is composed of a logarithmically compressor, a 2nd-order log domain filter core shown in Fig. 6.16 (a), and an exponential expander M_1 to M4. In Fig. 6.16 (a) its cutoff frequency Ω_c is tunable by V_c and a log domain operational transconductance amplifier (OTA) shown in Fig. 6.16 (b) is used in the master filter and the slave filter. MOSFETs M_1 to M_4 as an expander are also used as input devices of the mixer which is a balanced configuration and thus the mixer has high linearity. An output voltage of the log domain filter core is mixed with V_{in} by alternately switching two current paths: while one is through M_1 and M_3, another is through M_2 and M_4. Although floating switches driven by V_{in} are used in the mixer, a potential of a common bottom terminal is less
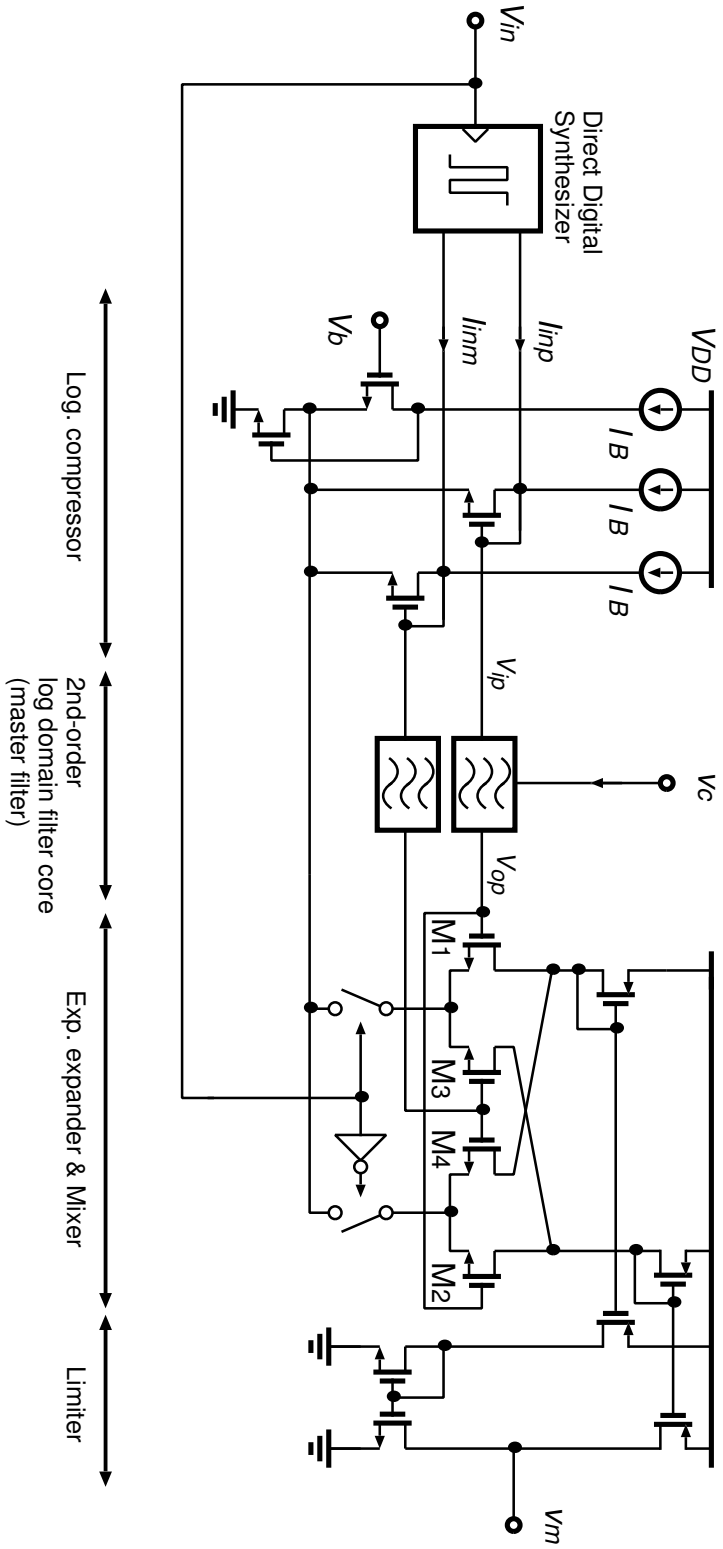
Figure 6.15: A master filter and a mixer including exponential expander.
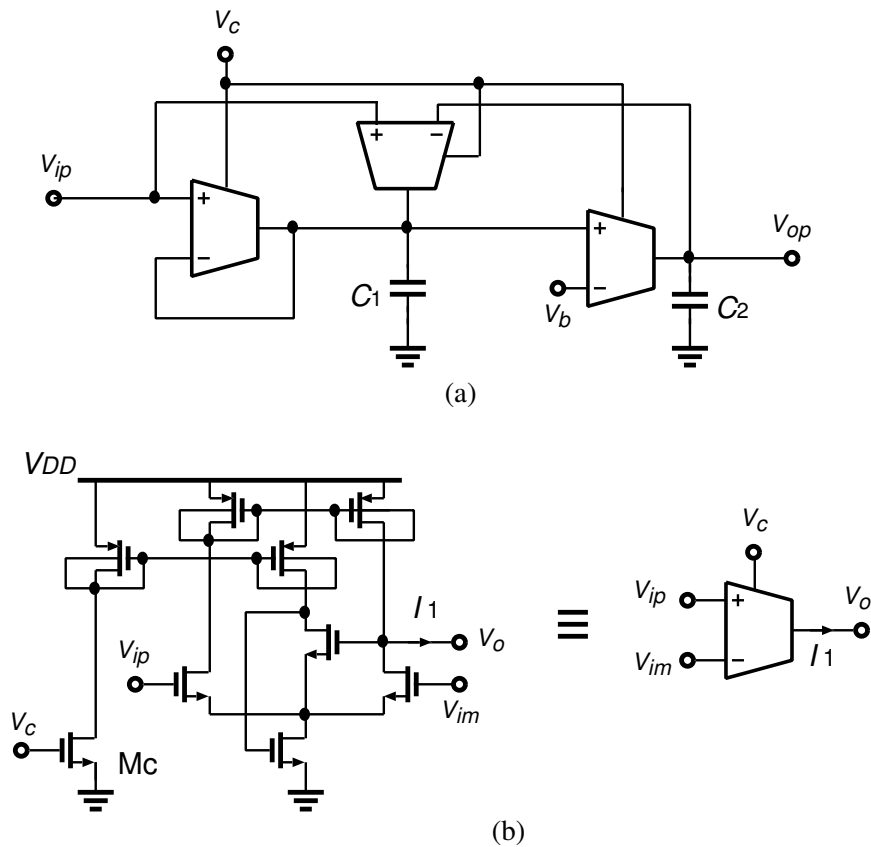
Figure 6.16: A second-order low-pass log domain filter core (one half only): (a) configuration and (b) a tunable log domain OTA.

than 0.1 V and thus these switches are realized by n-channel MOSFET and not detrimental for low-voltage operation. Eventually, an amplitude of the mixed signal is limited by a limiter. If the cutoff frequency of the master filter equals a frequency of V_{in}, the output voltage V_m becomes a pulse with 50-% duty ratio. In Fig. 6.14 a phase Φ_{out} of the pulse V_m is compared to a phase Φ_{in} of the reference clock V_{ref} by DRD, which has 50-% duty ratio. The DRD outputs two pulses, Up and Down, which drive the CP. For instance, consider a case that a delay of $\phi_0/2$ occurs for Φ_{out}, which means a degradation of the cutoff frequency of the main filter corresponding to a phase delay of ϕ_0 in the filter. The DRD detects the phase difference of ϕ_0 between Φ_{in} and Φ_{out} and outputs a high Up pulse during the period of ϕ_0. A capacitor C_p is charged by a constant current I_p and then V_c increases through a loop filter (LF). The
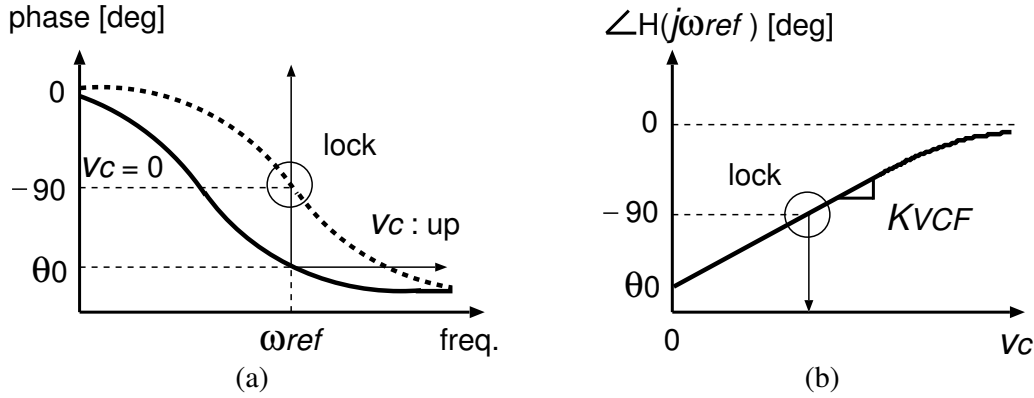
Figure 6.17: (a) phase response of the master filter $H_{mst}(s)$ and (b) relation between frequency shift and control voltage V_c.

LF is composed of passive elements, such as resistors or capacitors. Assuming that V_c is proportional to the cutoff angular frequency Ω_c of the main filter, Ω_c increases. If $\Omega_c = \omega_{ref}$, Φ_{out} is a pulse wave with 50-% duty ratio and the DRD does not output any pulses. Therefore, the proposed system shown in Fig. 6.14 can set Ω_c into a desired ω_{ref}.

6.4.2 Equivalent Linearized Model and Stability

An equivalent linearized model of the system shown in Fig. 6.14 is considered to analyze its stability. First, a relation between a control voltage V_C and a phase shift of the master filter is described. Since the main filter is a second-order biquad structure and then its transfer function $H_{mst}(s)$ is expressed as Eq. (6.12), a phase response of $H_{mst}(s)$ is sketched as in Fig. 6.17 (a). In this figure it is assumed that a cutoff angular frequency Ω_c of the master filter is proportional to a control voltage V_C and an initial value a phase delay for $V_C = 0$ is θ_0. If V_{in} is a cosine wave with an angular frequency ω_{ref}, the phase of the master filter output is expressed as

$$\arg H_{mst}(j\omega_{ref}) = -\tan^{-1} \frac{\dfrac{1}{Q}\dfrac{\omega_{ref}}{\Omega_c(V_c)}}{1 - \left[\dfrac{\omega_{ref}}{\Omega_c(V_c)}\right]^2} \tag{6.16}$$
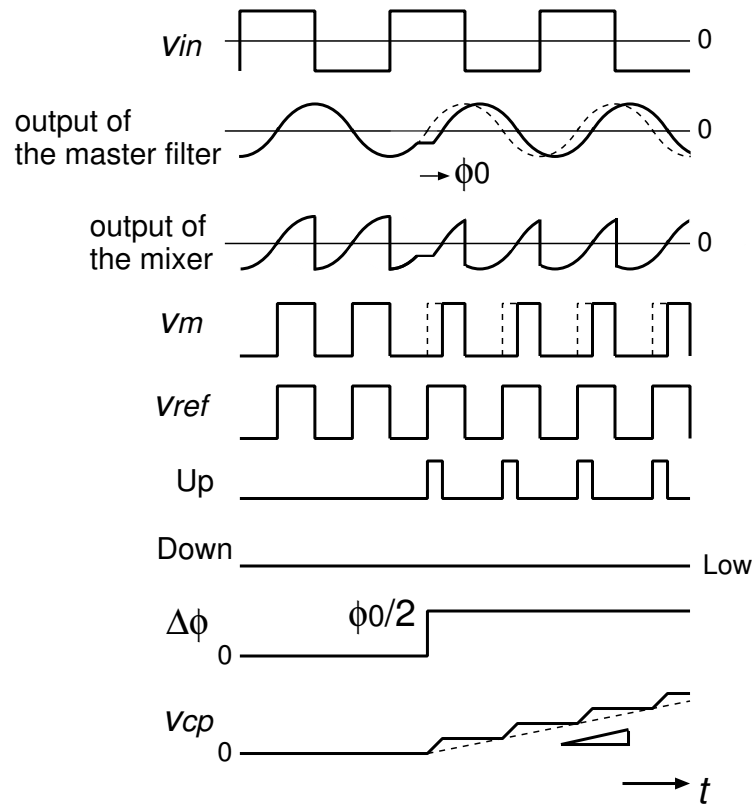
Figure 6.18: Control voltage and phase behavior when a cutoff frequency f_c changes.

and since this equation can be drawn as Fig. 6.17 (b) for a constant ω_{ref}, the first-order approximation of the phase delay for change of V_c is expressed as

$$\arg H_{mst}(j\omega_{ref}) \approx K_{VCF}V_c + \theta_0 \qquad (6.17)$$

where K_{VCF} is a voltage-to-phase conversion gain [rad/V] and depends on Q of the master filter: in general $Q = 1/\sqrt{2}$.

Next, a linearized model of the DRD and the CP is considered by using its step response. Figure 6.18 shows waveforms at each node in Fig. 6.14 when the cutoff frequency Ω_c steps out of a desired ω_{ref}. In this case if a phase delay ϕ_0 for the output of the master filter arises, then a delay for the output of the mixer becomes $\phi_0/2$. Therefore a phase difference between V_m and V_{ref}, $\Delta\phi = \phi_{in} - \phi_{out}$, also becomes $\phi_0/2$, which corresponds to a step input in phase domain. The DRD outputs 'Up' signal in $\phi_0/2$ with respect to a period of V_{ref} and then an output V_{cp} of the CP quasi
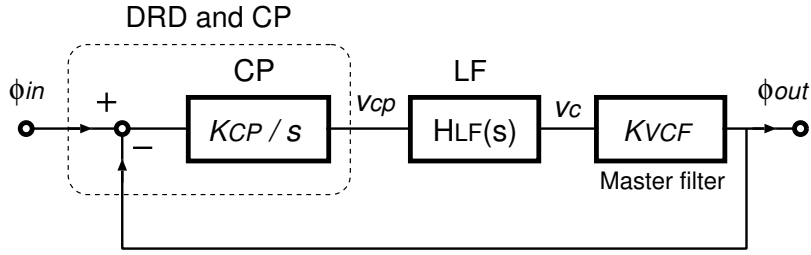
Figure 6.19: Linearized mode of the proposed frequency tuning system.
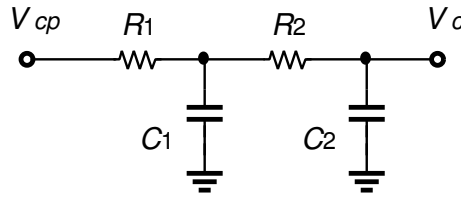
Figure 6.20: Loop filter $H_{LP}(s)$.

ramps up as shown in Fig. 6.18. Assuming that V_{cp} is purely ramp function for $\Delta\phi$, the output of CP is approximately expressed for time domain as

$$V_{cp} \approx \frac{I_p\phi_0}{4\pi C_p}t \tag{6.18}$$

and thus, as a transfer function from $\Delta\phi$ to V_{cp}

$$\frac{V_{cp}(s)}{\Delta\phi(s)} = \frac{I_p}{4\pi C_p} \cdot \frac{1}{s} \tag{6.19}$$

is provided. From the above equation it is confirmed that a combination of DRD and CP works as an integrator [31]. As a consequence, a linearized model of the tuning system shown in Fig. 6.14 is obtained as a block diagram of Fig. 6.19 in phase domain. In this figure $K_{CP} = I_p/(4\pi C_p)$ and $H_{LF}(s)$ is a transfer function of the LP.

Since the proposed frequency tuning system shown in Fig. 6.14 uses negative feed back loop, a stability must be checked and analyzed by utilizing a block diagram shown in Fig. 6.19. The LF is composed of resistors and capacitors as shown in Fig. 6.20 to suppress a ripple of V_{cp} and its transfer function $H_{LF}(s)$ is expressed as

$$H_{LF}(s) = \frac{1}{R_1R_2C_1C_2s^2 + (R_1C_1 + R_1C_2 + R_2C_2)s + 1}. \tag{6.20}$$

An open loop transfer function $H_{open}(s)$ of the block diagram shown in Fig. 6.19 becomes

$$
\begin{aligned}
H_{open}(s) &= \frac{K_{CP}}{s} \cdot H_{LF}(s) \cdot K_{VCF} \\
&= \frac{K_{CP}K_{VCF}}{R_1R_2C_1C_2s^3 + (R_1C_1 + R_1C_2 + R_2C_2)s^2 + s}
\end{aligned}
$$

and thus, a closed loop transfer function $H_{closed}(s)$ is given as

$$
\begin{aligned}
H_{closed}(s) &= \frac{H_{open}(s)}{1 + H_{open}(s)} \\
&= \frac{K_{CP}K_{VCF}}{R_1R_2C_1C_2s^3 + (R_1C_1 + R_1C_2 + R_2C_2)s^2 + s + K_{CP}K_{VCF}}.
\end{aligned}
$$

Since a characteristic equation of $H_{close}(s)$ is

$$
R_1R_2C_1C_2s^3 + (R_1C_1 + R_1C_2 + R_2C_2)s^2 + s + K_{CP}K_{VCF} = 0,
$$

the Hurwitz's matrix H is given by

$$
H = \begin{bmatrix}
R_1C_1 + R_1C_2 + R_2C_2 & K_{CP}K_{VCF} & 0 \\
R_1R_2C_1C_2 & 1 & 0 \\
0 & R_1C_1 + R_1C_2 + R_2C_2 & K_{CP}K_{VCF}
\end{bmatrix}.
$$

From the matrix three conditions are provided as follows:

$$
\begin{aligned}
H_1 &= R_1C_1 + R_1C_2 + R_2C_2 > 0 \\
H_2 &= R_1C_1 + R_1C_2 + R_2C_2 - R_1R_2C_1C_2K_{CP}K_{VCF} > 0 \\
H_3 &= K_{CP}K_{VCF} \times H_2 > 0.
\end{aligned}
$$

Therefore required conditions for stability are given as

$$
\begin{aligned}
R_1C_1 + R_1C_2 + R_2C_2 &> R_1R_2C_1C_2K_{CP}K_{VCF} \\
K_{VCF} &> 0.
\end{aligned}
$$

For example, in Fig. 6.16 (a) the designed master filter has K_{VCF} of $\pi/2$ and the parameters of the LF in Fig. 6.20 are determined as follows: $R_1 = R_2 = 1.0$ MΩ,

$C_1 = 20$ pF, and $C_2 = 10$ pF. In the CP $I_p = 1.0$ μA and $C_p = 10$ pF and thus $K_{CP} = 10^5/(4\pi)$ [V/rad]. In this case since $K_{VCF} > 0$ and inequality expressions

$$4 \times 10^{-5} > 200 \times 10^{-12} \times \frac{10^5}{4\pi}\frac{\pi}{2} = 2.5 \times 10^{-6}$$

are satisfied, it is confirmed that the negative feedback loop of the designed frequency tuning system is stable.

6.5   Conclusion

Low-voltage biasing circuits are proposed in this chapter for syllabic companding log domain filters. The control current generator is realized by use of the proposed low-voltage current peak detector using the equivalent diode circuit. The prototype chip of the detector in 0.35-μm CMOS technology is measured and has wide-detection range at a power supply of 0.8 V. As another solution for the generator, three-value quantized envelope detector to suppress a ripple is described. The voltage reference circuit using p-channel MOSFETs in weak inversion region is also proposed. The simulated results shows the circuit has a temperature coefficient of -25.5 ppm/C$^\circ$ at 27 C$^\circ$. Its prototype chip in 0.18-μm CMOS technology is measured at room temperature and outputs 0.4 V from a power supply of 0.55 V. Finally, the low-voltage frequency tuning system based on a voltage-controlled filter technique is proposed. The system utilizes a duty ratio detector and a charge pump circuit instead of a high-gain amplifier for low-voltage operation. Furthermore, by combining a master filter with a mixer, highly linear signal processing is realized. Stability of the system is also analyzed by Hurwitz's stability criterion.

Chapter 7

Measured Results of the Prototype Chips

7.1   Introduction

Two 5th-order Chebychev low-pass filters with 100-kHz cutoff frequency are designed by use of the proposed low-voltage syllabic companding technique and the measured results are shown in this chapter. One of them is fabricated in a 0.35-μm CMOS technology and uses the current-type state variable correction (SVC) method. The other with the voltage-type SVC method is done in a 0.18-μm CMOS technology and includes the low-voltage frequency tuning system and the voltage reference circuit described in Chapter 6. Characteristics of the latter filter is compared to other recently published filters and its effectiveness is confirmed by use of well known figure of merit (FOM).

Table 7.1: Transconductance and capacitances in a log domain filter core.

$G_m = \dfrac{I_0}{nU_T}$	51.0 μS
C_1, C_3	73.1 pF
C_4, C_5	48.7 pF
C_2	97.4 pF

7.2   5$^{\text{th}}$-order Chebychev Log Domain Filter in 0.35-μm CMOS

A designed 5$^{\text{th}}$-order Chebychev low-pass log domain filter is shown in Fig. 7.1 where a current-type SVC method is applied [84]. Transforming an RLC prototype ladder filter shown in Fig. 7.1 (b) by leap-frog simulation as described in Appendix A, a half circuitry of the 5$^{\text{th}}$-order log domain filter core shown in Fig. 7.1 (c) is obtained. In this design the 5$^{\text{th}}$-order Chebychev low-pass filter with a 100-kHz cutoff frequency and 0.5-dB ripple is considered as an application example. SVC currents I_{SVCi} equal $nU_T C_i (dI_g/dt)/I_g$ for each integer i. All transconductors are identical and I_0 equals 1.5 μA in this design. Then each small-signal transconductance $G_m = I_0/(nU_T)$ and required capacitances should be as written in Table 7.1.

The best SNDR curve of the DAB-based filter is provided by an optimum control current I_g as discussed in Chapter 5, which is obtained by use of an ideal envelope detector. However, since a practical envelope detector generates a slight ripple as well to induce an output distortion of a filter, the control current I_g is discretely varied to avoid the disturbance [54], [62]. In this case a piece-wise constant control current generator is suitable, which is proposed in Chapter 6 and a circuit depicted in Fig. 7.2 is used here. I_g takes I_{ref1} or $I_{ref1} + I_{ref2}$ through a switch S_W which is controlled depending on the input current amplitude I_{env}. If I_{env} is less than a threshold current I_{th}, then $I_g = I_{ref1}$. Otherwise, $I_g = I_{ref1} + I_{ref2}$. A MOSFET M$_{\text{F}}$ in triode region and a capacitor C_F compose a low-pass filter for avoiding a sharp edge of I_g which makes an SVC current infinite theoretically as seen from Eq. (4.11). An SNDR obtained by use of this control circuit is examined. The simulated SNDR

Figure 7.1: Syllabic-companding log domain fifth-order Chebychev low-pass filter: (a) overall circuity, (b) RLC prototype filter, and (c) log domain filter core (one half only).

curves of the filter are shown by the dashed lines in Fig. 7.3 for cases of $I_g = 2.0$ μA and $I_g = 20$ μA. Two curves intersect at about 1-μA input. For I_g less than 2 μA a sufficient frequency response cannot be obtained due to a parasitic capacitance at the input terminal of the filter. On the other hand, if I_g is greater than about 20 μA, a peak of SNDR decreases due to a large distortion resulting from unintended operation region of MOSFETs. Therefore in this design the bias currents I_{ref1}, I_{ref2}, and the

Figure 7.2: Control current I_g generator.
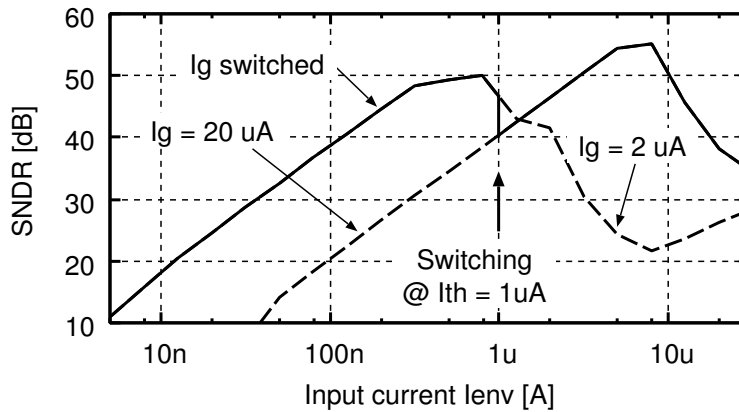
Figure 7.3: Simulation results of signal-to-noise-plus-distortion ratios (SNDRs) for a 100-kHz sinusoidal input current.

threshold current I_{th} are determined as 2 μA, 18 μA, and 1 μA, respectively. The expected SNDR characteristic of the filter controlled by this I_g generator is depicted as a solid line of Fig. 7.3, that is crossover of two dashed lines.

The prototype filter was fabricated in a 0.35-μm CMOS technology and its microphotograph is shown in Fig. 7.4. A circuit controlling S_W is not implemented on this chip due to insufficient area. The area of the filter is 1.4 mm $\times$ 1.6 mm. The proposed filter operates at a power supply of 0.8 V. The measurement setup is shown in Fig. 7.5 in which voltage-to-current and current-to-voltage converters consisting of
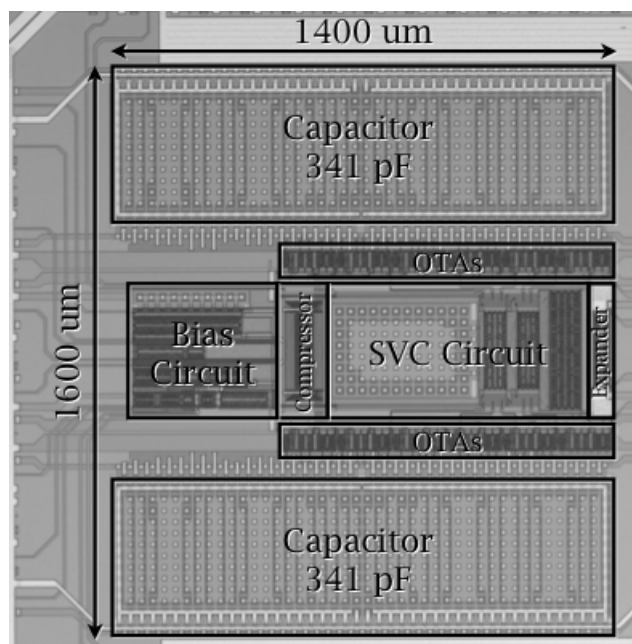
Figure 7.4: Chip microphotograph.
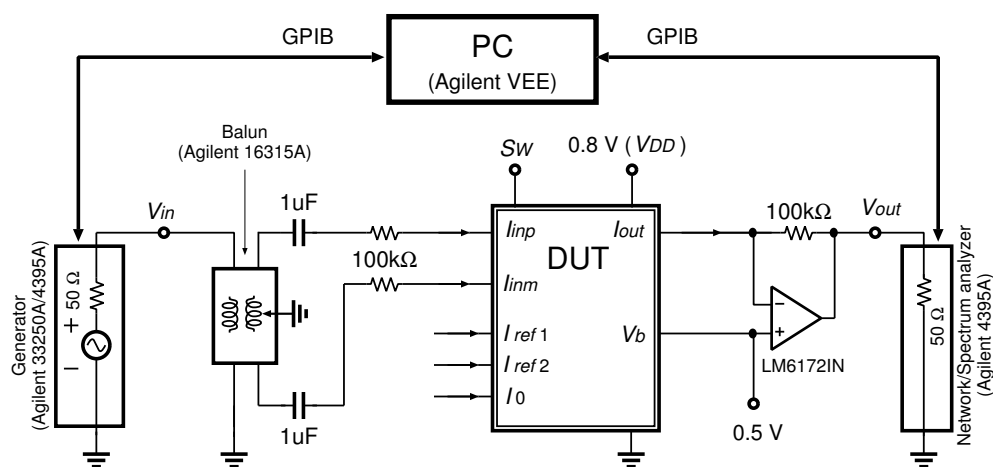
Figure 7.5: Measurement setup.

off-chip resistors and an operational amplifier are used.

The frequency response of the filter is shown in Fig. 7.6. The curve meets to the ideal response well in a range less than 200 kHz when $I_g = 20$ μA. Although the passband gain for $I_g = 2$ μA is about 4 dB lower than the ideal one, the cutoff
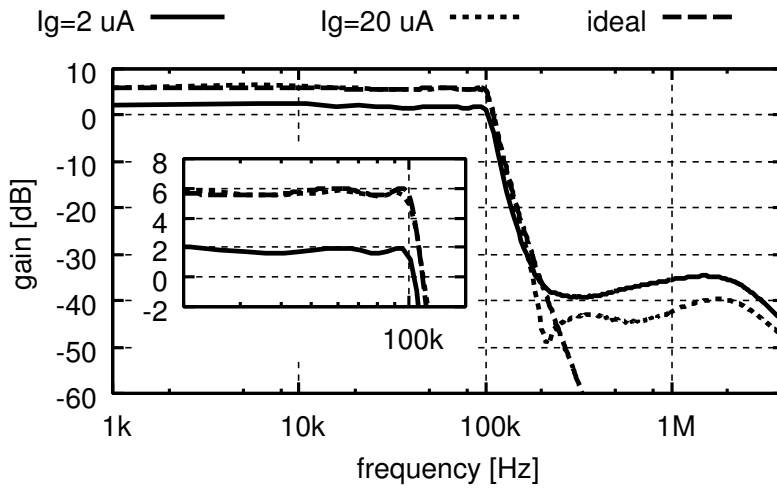
Figure 7.6: Measured frequency responses.
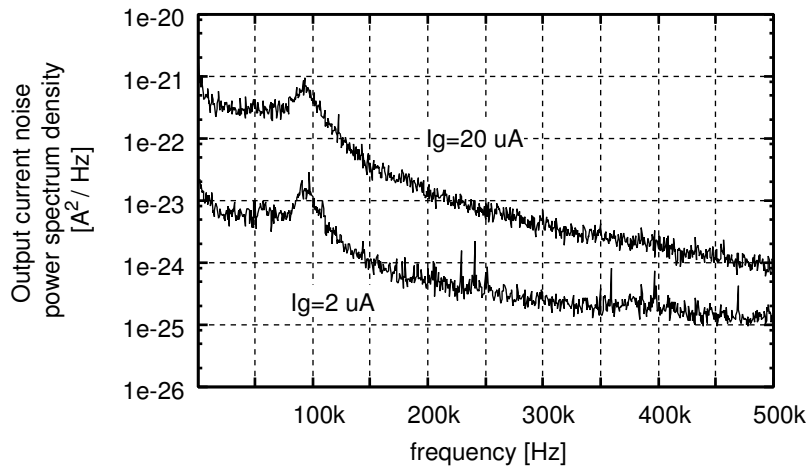
Figure 7.7: Measured output noise current power spectrum density.

frequency of the filter equals to 100 kHz. In results of SPICE simulation, the passband gain for each I_g is 6 dB for $I_g = 2$ μA as well as 20 μA. The degradation of the passband gain at $I_g = 2$ μA may be attributed to the change of the input or output impedance of the filter, which is varied by the control current I_g. The stopband attenuation is smaller than the ideal one. The output current noise power spectrum density (PSD) is shown in Fig. 7.7. It can be verified that the noise PSD becomes low when the control current is small. The output noise RMS currents over the band
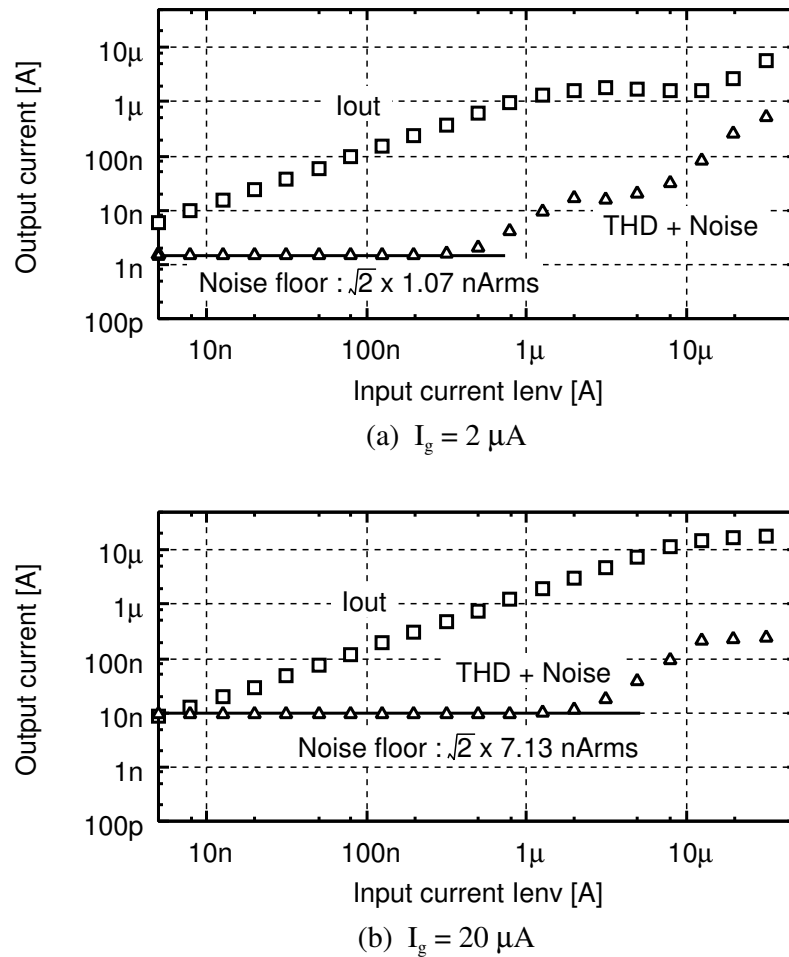
Figure 7.8: Output current components with a 100-kHz sinusoidal input current amplitude varied.

up to 500 kHz for 2-μA and 20-μA I_g's are 1.07 and 7.13 nA$_{\mathrm{rms}}$, respectively.

Figure 7.8 (a) shows the output fundamental component I_{out} and RMS of the total of noise and harmonic distortion for a 100-kHz sinusoidal input current I_{in} when $I_g = 2$ μA and (b) does those when $I_g = 20$ μA. The maximum input current amplitude under -40-dB total harmonic distortion (THD) is about 2 μA for $I_g = 2$ μA and 9 μA for I_g=20 μA. The SNDR of the filter obtained from Fig. 7.8 is shown in Fig. 7.9. Since the threshold current I_{th} for switching I_g in Fig. 7.2 is set as 1 μA, the two SNDR curves of Fig. 7.9 are appropriately switched by according to the input current amplitude. The dynamic range is 78 dB which is calculated by

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input current : 100-kHz sinusoid
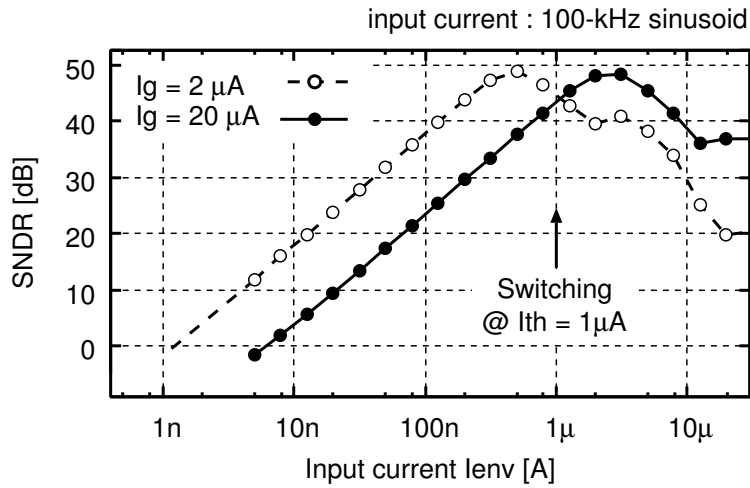
Figure 7.9: Signal to noise plus distortion ratios for a 100-kHz sinusoidal input current.

$20 \log[I_{out,max}/(\sqrt{2} \cdot I_{on,min})]$ where $I_{out,max}$ is an output current under -40-dB THD when $I_g = 20$ μA and $I_{on,min}$ be an output current noise when $I_g = 2$ μA.

The output current waveforms when I_g changes are shown in Fig. 7.10. The input current is a 20-kHz sinusoidal current with 500-nA amplitude. A distortion of the output waveforms I_{out} is not clearly observed. It is confirmed that the ELTI relation between input and output is almost kept by the proposed current-type SVC circuit shown in Fig. 4.4 (c).

A performance summary of the filter is given in Table 7.2. The power consumption is 200 μW from a 0.8-V power supply. Finally, comparison with other low-voltage analog filter recently reported is summarized in Table 7.3.
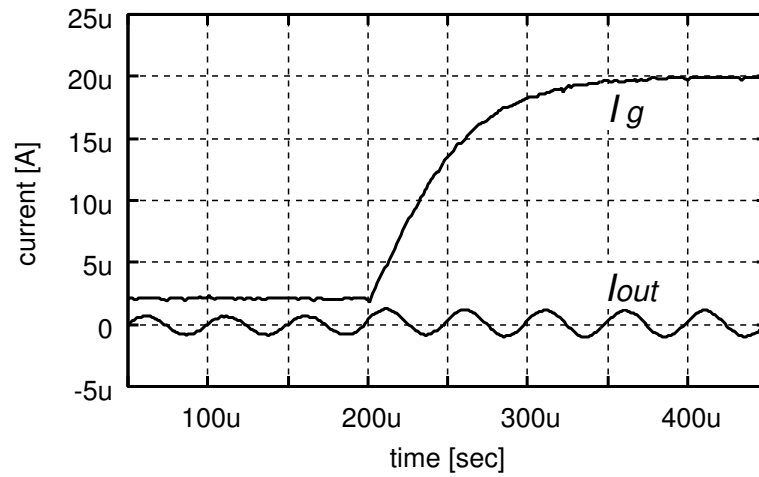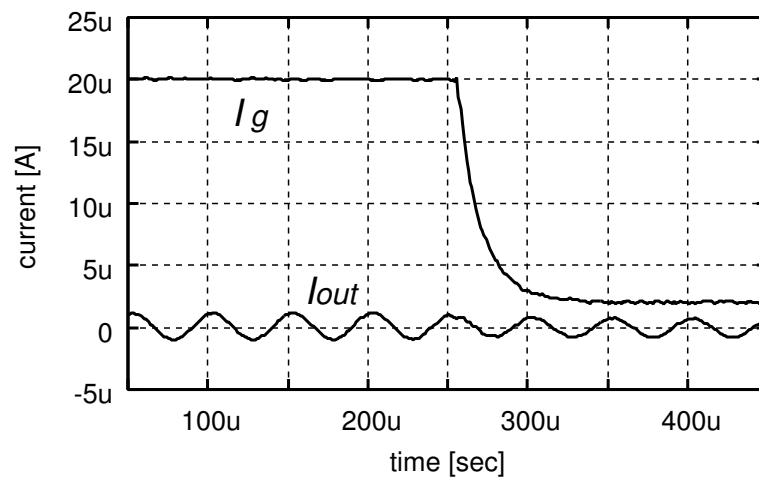
Figure 7.10: Output current waveforms with I_g varied when a 20-kHz sinusoidal input current applied.

Table 7.2: Summary of measured filter characteristics.

Order and type	5th-order Chebychev	
	0.5 dB ripple	
Technology	0.35-μm standard CMOS	
Cutoff frequency	100 kHz	
Supply voltage	0.8 V	
Active area	1.4 mm $\times$ 1.6 mm	
Dynamic range		
@ $I_{in} = 10$ kHz	85 dB	
@ $I_{in} = 100$ kHz	78 dB	
Control current I_g	2 μA	20 μA
Power Dissipation	91 μW	200 μW
Stopband attenuation	-37 dB	-46 dB
Output current noise	1.07 nA$_{\text{rms}}$	7.13 nA$_{\text{rms}}$

Table 7.3: Comparison with other low-voltage filters.

	[16]	[54]	This work
Supply voltage	0.5 V	1.2 V	0.8 V
Technology	0.18 μm	0.18 μm	0.35 μm
	CMOS	CMOS	CMOS
Power	1.1 mW	2.67 mW	200 μW
Cutoff frequency	135 kHz	100 kHz	100 kHz
Order	5	5	5
Dynamic Range	56.6 dB	80 dB	78 dB
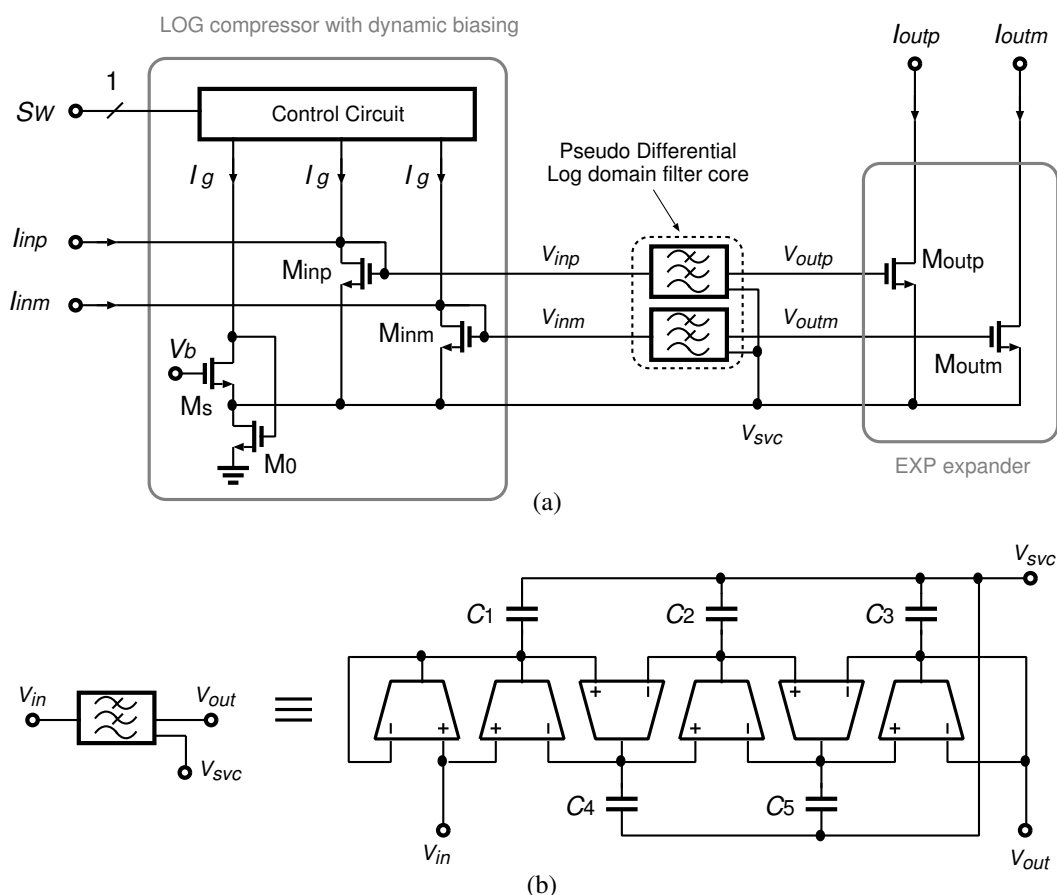
Figure 7.11: Syllabic-companding log domain fifth-order Chebychev low-pass filter using voltage-type SVC method: (a) overall circuity, (b) log domain filter core (one half only).

7.3   5$^{\text{th}}$-order Chebychev Log Domain Filter in 0.18-μm CMOS

A designed 5$^{\text{th}}$-order Chebychev low-pass log domain filter using a 0.18-μm CMOS technology is shown in Fig. 7.11 (a), and a half of the log domain filter core is done in (b) where the voltage-type SVC method is applied. The overall filter circuitry is composed of a logarithmic (LOG) compressor, a log domain filter core, and an exponential (EXP) expander. The capacitances of the filter core are set to have a 100-kHz cutoff frequency and a 0.5-dB passband ripple like as the filter in a 0.35-μm CMOS process.

Figure 7.12 shows an overall block diagram of the prototype filter chip in which
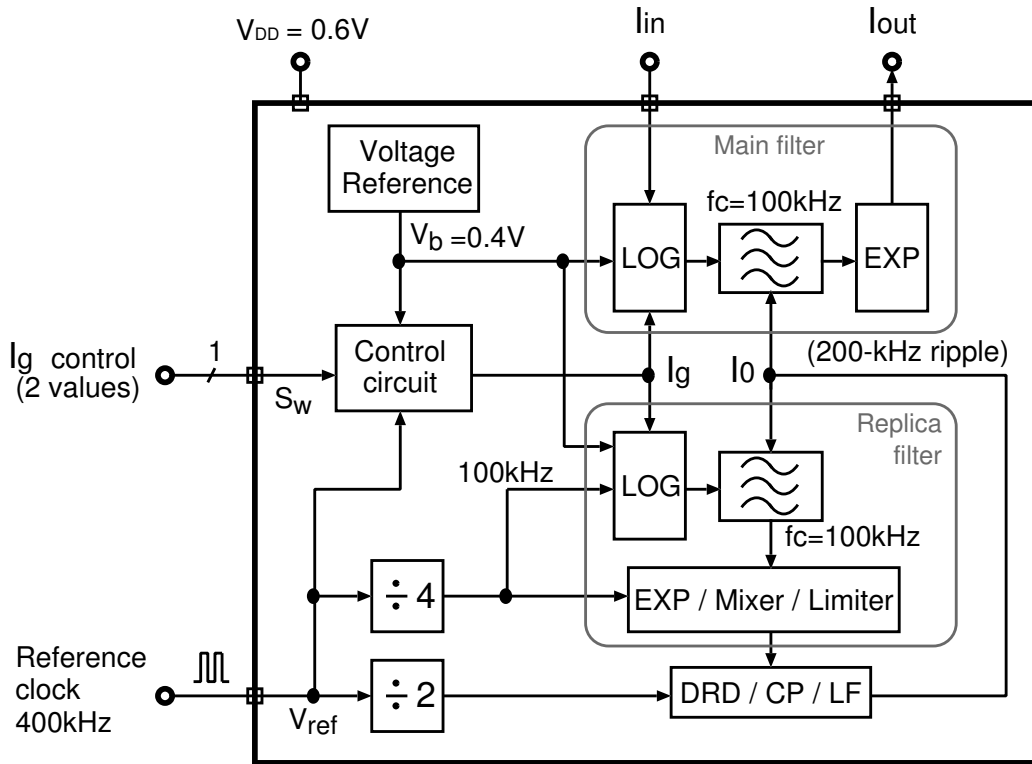
Figure 7.12: Overall block diagram of the prototype fitter chip.

a voltage reference circuit and a frequency tuning system are also integrated with the main filter shown in Fig. 7.11. The configuration of the reference circuit shown in Fig. 6.8 is used here, which outputs a bias voltage V_b of 0.4 V from a 0.6-V power supply for a wide range of temperature. For a control circuit in Fig. 7.12 a piece-wise constant current generator shown in Fig. 6.7 (a) is applied. The control current I_g is varied by a one-bit signal, named as "I_g control S_W," with smooth slope as shown in Fig. 6.7 (b). Each bias current weighted with different values in Fig. 6.7 (a) is generated by use of a constant bias voltage V_b. I_g takes I_{ref1} or $I_{ref1} + I_{ref2}$ through a switch S_W which is controlled depending on the input current amplitude I_{in}. If I_{in} is less than a threshold current , then $I_g = I_{ref1}$. Otherwise, $I_g = I_{ref1} + I_{ref2}$. In this design, $I_{ref1} = 5.0$ μA and $I_{ref2} = 45$ μA are chosen. For adjusting a cutoff frequency of the filter to a desired one, which is equal to 100 kHz in this design, a replica filter is used. The replica is composed of a LOG compressor, a 2nd-order log

domain filter core, and an EXP expander in Fig. 7.12. The filter core is synthesized by log domain operational transconductance amplifiers (OTAs) shown in Fig. 4.3 (b) and then its transconductance is proportional to a bias current I_0. Therefore a negative feedback around the replica filter, dividers, and a block of DRD/CP/LF generates an appropriate bias current I_0 to set a 100-kHz cutoff frequency. The tuning system is described in Chapter 6 and its detailed configuration is shown in Figs. 6.14 and 6.15. The prototype filter chip does not need any external elements, such as other bias circuits or resistors out of the chip, except for a 400-kHz reference clock and a one-bit signal for changing I_g. Therefore it can be said that the designed filter has highly integration.

The prototype filter was fabricated in a 0.18-μm CMOS technology and its microphotograph is shown in Fig. 7.13. The active area of the filter including a voltage reference circuit is 2.128 mm^2. The proposed filter operates at a power supply of 0.6 V. The measurement setup is shown in Fig. 7.14 in which voltage-to-current and current-to-voltage converters consisting of off-chip resistors and an operational amplifier are used. The inherent noise level of the setup in Fig. 7.14 is 106 pA$_{\text{rms}}$.

The frequency responses of the filter are shown in Fig. 7.15. The responses for each control current, $I_g = 5$ μA and 50 μA, agree except for a slight-ripple difference at the passband. In Fig. 7.15 the common-mode responses are also shown and its common-mode rejection ratios (CMRRs), which is a ratio of the frequency response to common-mode response, are greater than 26 dB for $I_g = 5$ μA and 31 dB for $I_g = 50$ μA. Figure 7.16 shows the phase and group delay characteristics for the different control current I_g. Although the phase for $I_g = 5$ μA is delayed compared to that for $I_g = 50$ μA, their group delay characteristics accord well. The output current noise PSD is shown in Fig. 7.17. It can be verified that the noise PSD becomes low when the control current is small. The output noise RMS currents over the band up to 500 kHz for 5-μA and 50-μA I_g's are 575 pA$_{\text{rms}}$ and 4.36 nA$_{\text{rms}}$, respectively.

Figure 7.18 (a) shows the output fundamental component I_{out} and RMS of
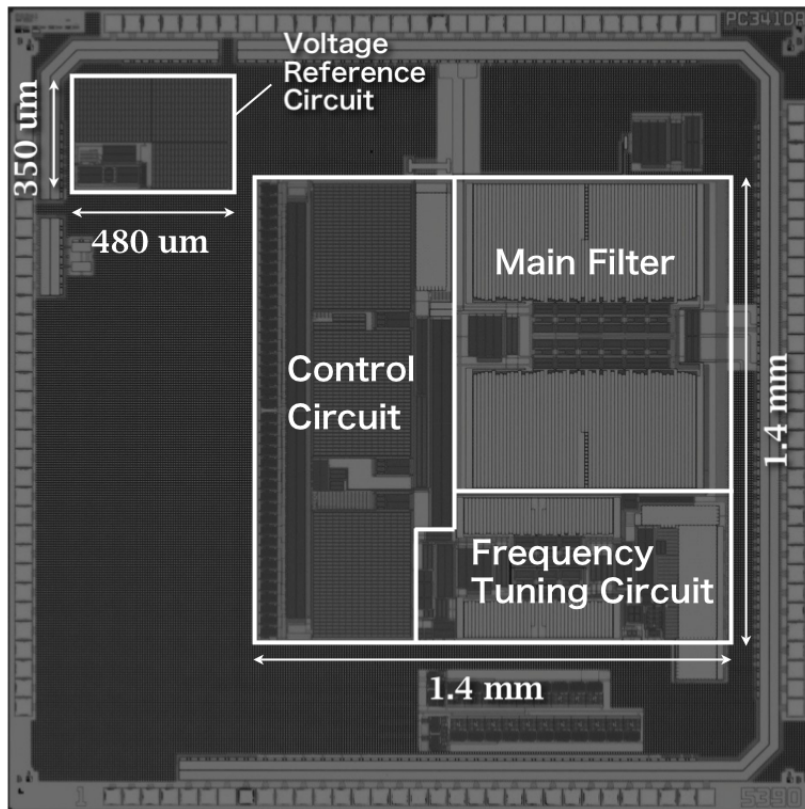
Figure 7.13: Chip microphotograph of the prototype filter in 0.18-μm CMOS.
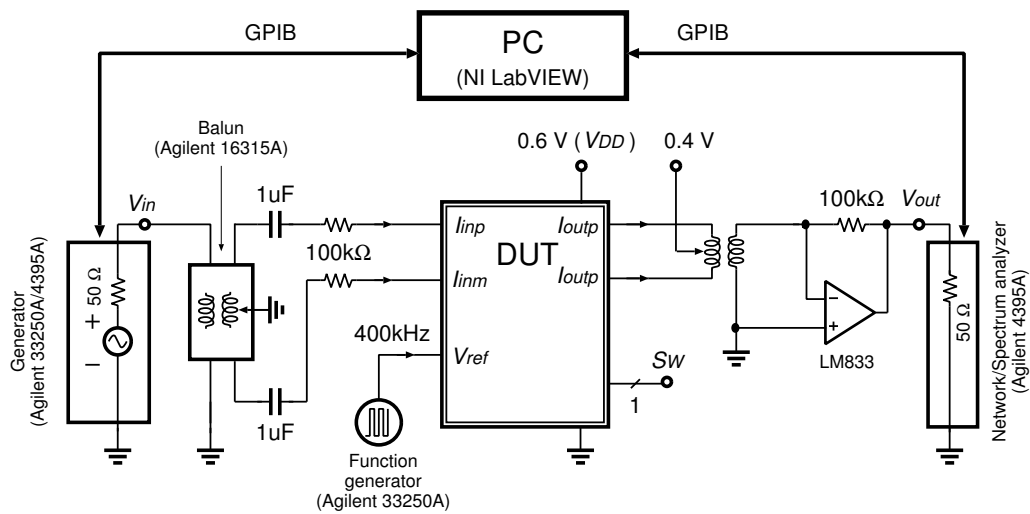
Figure 7.14: Measurement setup.
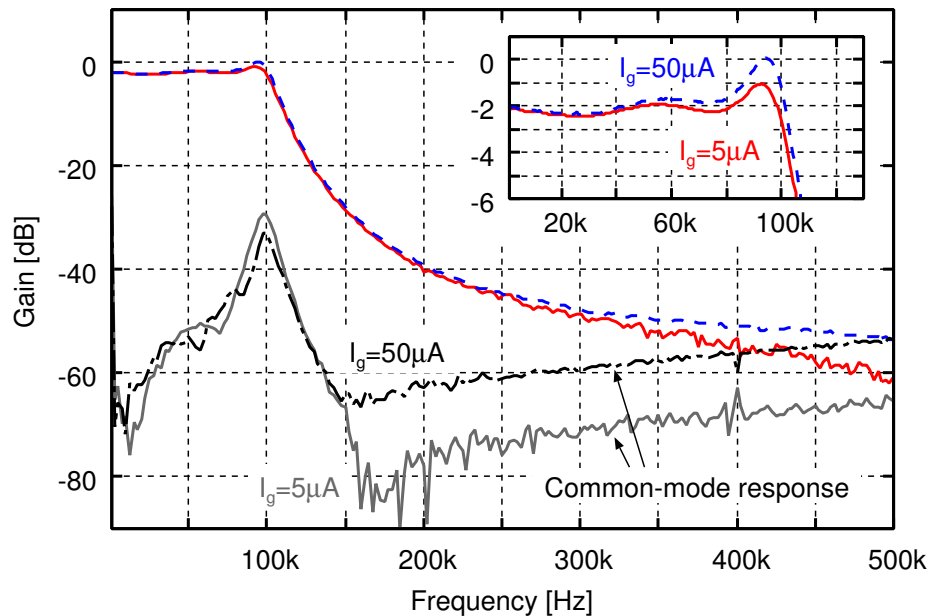
Figure 7.15: Frequency response and common-mode response at different control currents.

the total of noise and harmonic distortion for a 100-kHz sinusoidal input current I_{in} when $I_g = 5$ μA and (b) does those when $I_g = 50$ μA. The maximum input current amplitude under -40-dB THD is about 4 μA for $I_g = 5$ μA and 30 μA for $I_g=50\mu$A. The SNDR of the filter obtained from Fig. 7.18 is shown in Fig. 7.19. Figure 7.20 shows the results of a two-tones test where 40-kHz and 60-kHz sinusoidal input currents are applied to the filter. In this case the undesired signals, 20 and 80-kHz tones, as a third-order intermodulated distortion (IMD$_3$) are observed in an output of the filter. The input referred intercept points (IIP$_3$'s) for each I_g are 14 μA and 188 μA as seen from Fig. 7.20, which are obtained from an input-referred point at the intersection of extrapolated lines for the fundamental and the IMD$_3$ components [76]. Concerning with an out-of-band IIP$_3$'s for 220-kHz and 380-kHz tones, 3.4 μA and 74.5 μA are obtained at $I_g = 5$ μA and 50 μA, respectively. Furthermore, the dynamic range of the prototype filter for a 100-kHz sinusoidal input current is 89 dB which is calculated by $20 \log[I_{out,max}/(\sqrt{2} \cdot I_{on,min})]$ where $I_{out,max}$ is an output current under -40-dB THD when $I_g = 50$ μA and $I_{on,min}$ be an output
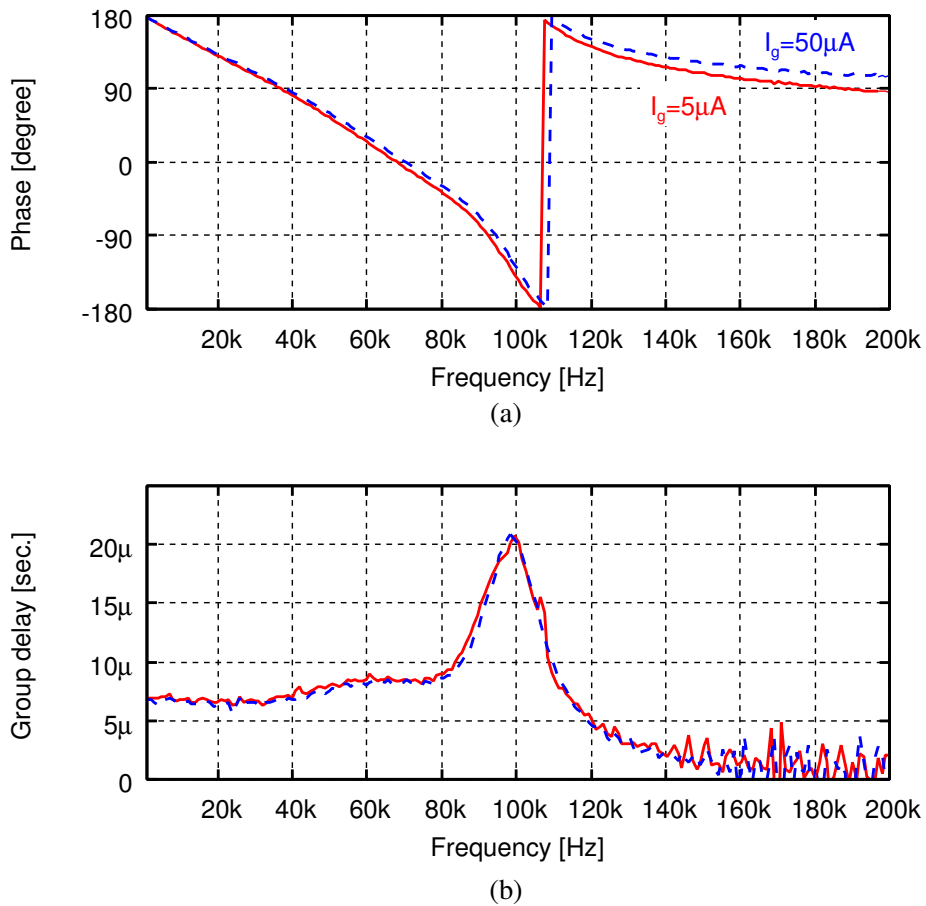
Figure 7.16: Phase and group delay characteristics.
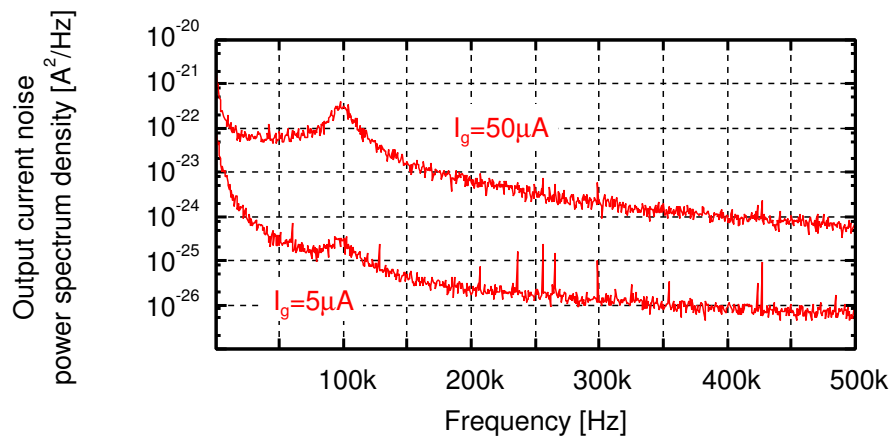
Figure 7.17: Output current noise power spectrum density at different control currents.
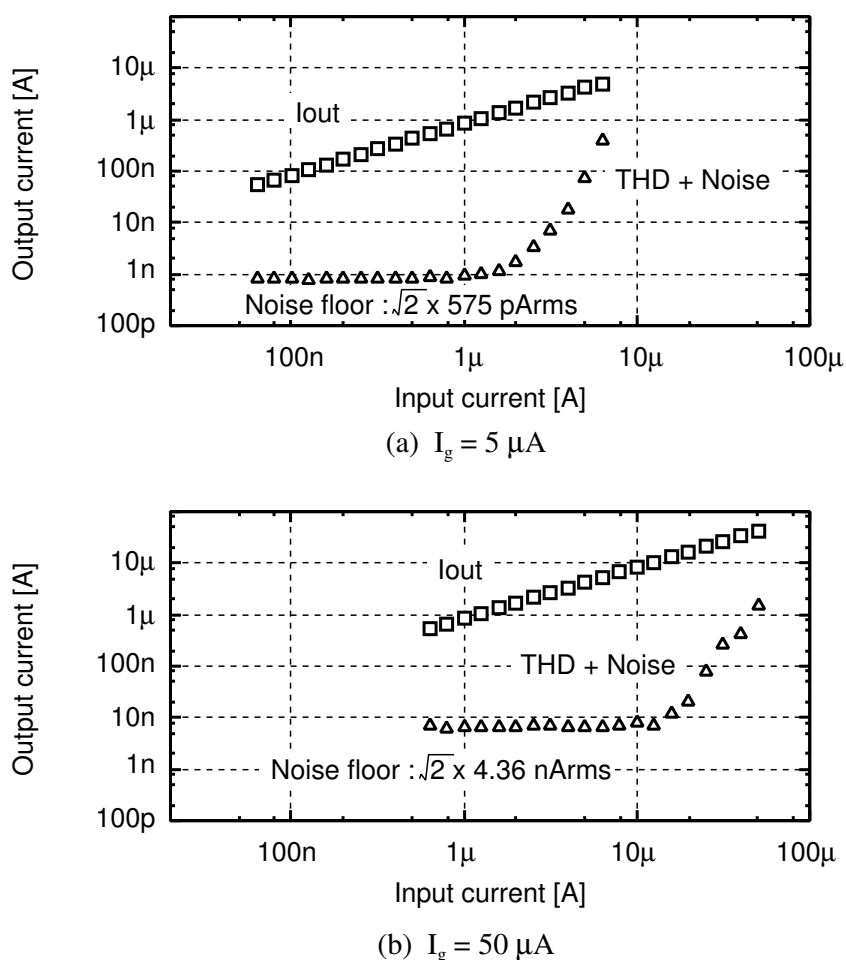
Figure 7.18: Output current components with a 100-kHz sinusoidal input current amplitude varied.

current noise when $I_g = 5$ μA.

The output current waveforms with I_g changes are shown in Fig. 7.21 where a 50-kHz sinusoidal current with an amplitude of 4-μA is applied. Figure 7.21 (a) shows the simulated waveforms when the voltage-type SVC method does not used. As seen from the results the output current I_{out} is influenced by change of I_g. On the other hand, the measured output current waveforms of the filter chip, which uses the SVC scheme, are shown in Fig. 7.21 (b) and then it is confirmed that a disturbance for the waveforms due to change of I_g is suppressed in comparison to the simulated waveforms without SVC. Therefore the filter has the ELTI relation between the input

input current : 100-kHz sinusoid

SNDR [dB]

$I_g = 2\ \mu A$ ○

$I_g = 20\ \mu A$ ●

70
60
50
40
30
20
10
0
-10

1n   10n   100n   1μ   10μ   100μ
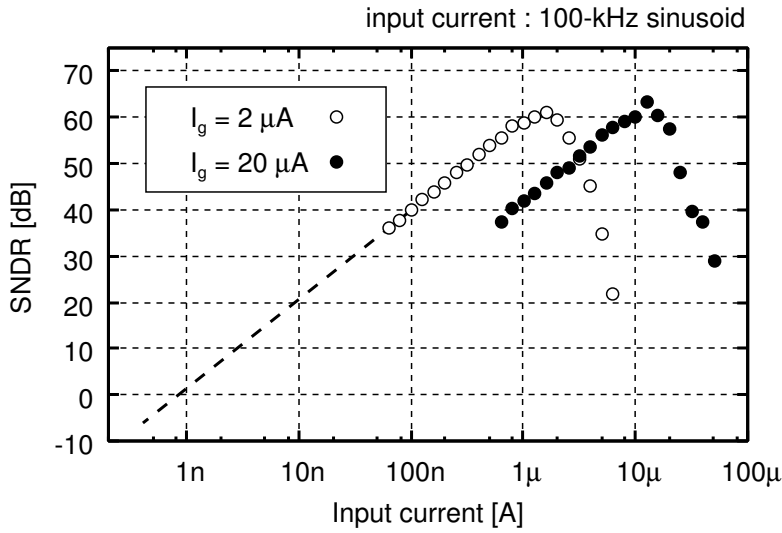
Input current [A]

Figure 7.19: Signal-to-noise-plus-distortion ratios (SNDRs) for a 100-kHz sinusoidal input current.

IIP_3 :14uA@I_g=5uA IIP_3 :188uA@I_g=50uA

Output current [A]

100u
10u
1u
100n
10n
1n
100p

● I_{out} @ I_g=5μA

▲ IMD_3 @ I_g=5μA

○ I_{out} @ I_g=50μA

▽ IMD_3 @ I_g=50μA

100n   1u   10u   100u

Input curret [A]
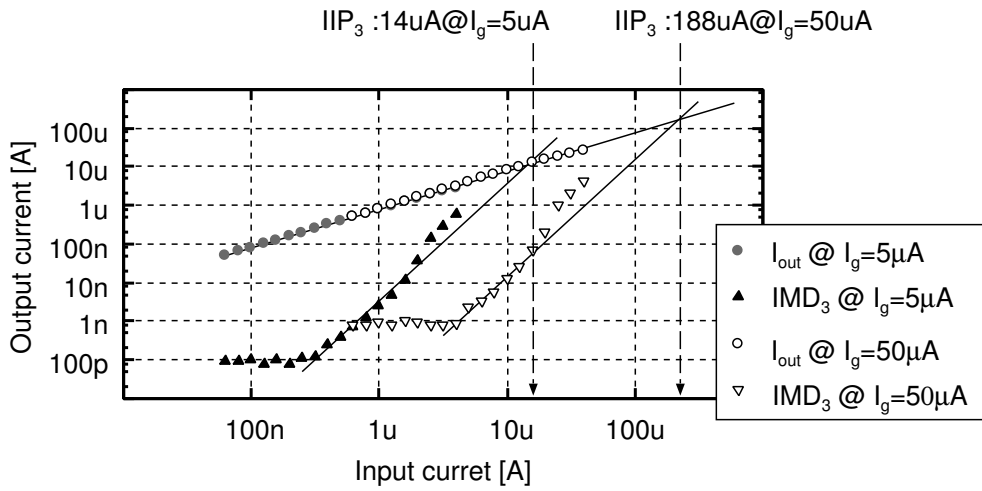
Figure 7.20: Fundamental components and third-order intermodulated distortions (IMD_3) and third-order in-band input-refereed intercept point (IIP_3) for each I_g where 40-kHz and 80-kHz tones are applied.

and the output.

A performance summary of the filter is given in Table 7.4. The power consumption is 443 μW from a power supply of 0.6 V.

(a) without SVC connection (simulated)
 – Disturbance arises due to changing I$_g$.

(b) with SVC connection (measured)
 – Disturbance is suppressed by SVC.
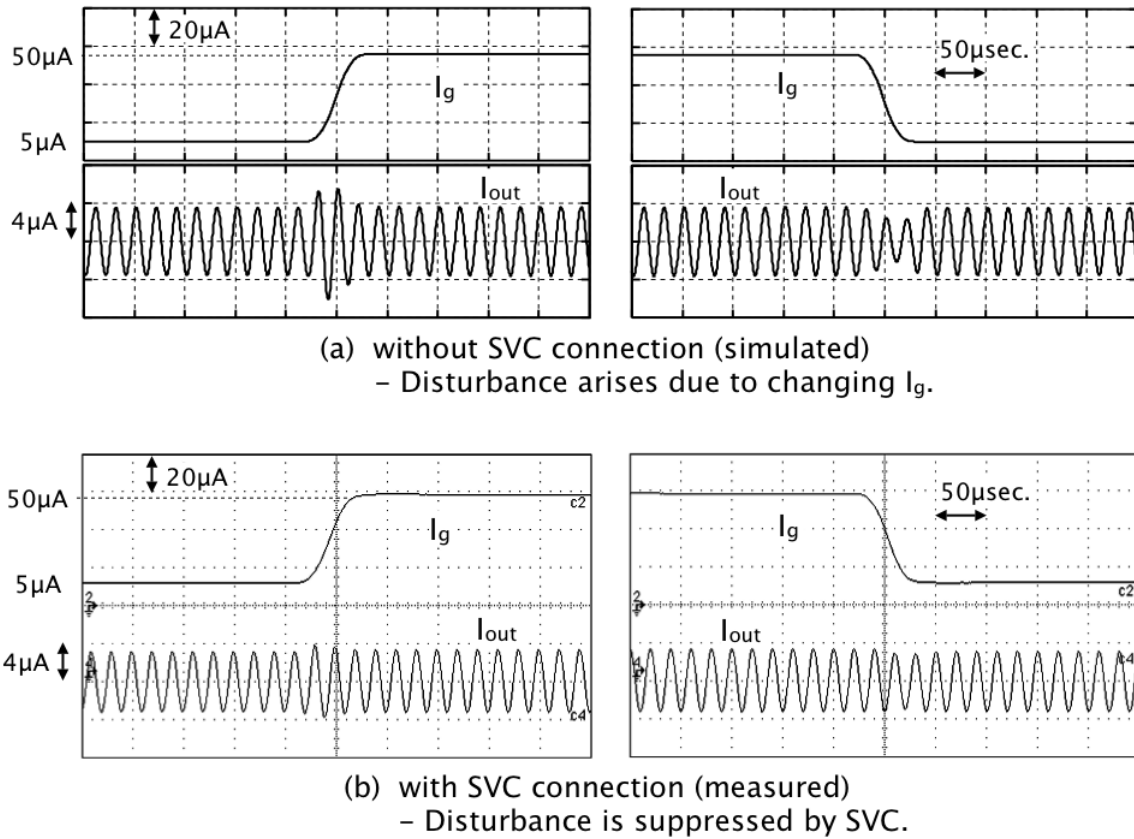
Figure 7.21: Transient response when the control current I_g changes: (a) simulated results without SVC and (b) measured results with SVC.

Table 7.4: Performance summary.

Order N and filter type		5th-order Chebychev
		0.5 dB ripple
Technology		0.18-μm standard CMOS
Cutoff frequency f_c		100 kHz
Supply voltage V_{DD}		0.6 V
Dynamic range @ -40 dB THD	10kHz tone	94 dB
	100kHz tone	89 dB
Active area		2.128 mm^2
Control current I_g	5 μA	50 μA
Power Dissipation	217 μW	443 μW
Common-mode rejection ratio	> 26 dB	> 31 dB
In-band IIP$_3$ @ 40kHz and 60kHz tones	14 μA	188 μA
Out-of-band IIP$_3$ @ 220kHz and 380kHz tones	3.4 μA	74.5 μA
Output noise (1kHz to 500kHz)	575 pA$_{\text{rms}}$	4.36 nA$_{\text{rms}}$

7.4   Comparison to Conventional Filters

The prototype filter in a 0.18-μm CMOS technology is compared to other recently published filters in the viewpoint of a relation between a supply voltage and a figure of merit (FOM). The FOM is calculated from

$$\text{FOM} = \frac{\text{power consumption [W]}}{N \times \text{BW [Hz]} \times \text{DR}_{\text{OIP}_3}} \ \text{[J]} \tag{7.1}$$

where N and BW mean the number of pole and band width of filters, respectively. A dynamic range DR_{OIP_3} for FOM is given by

$$\text{DR}_{\text{OIP}_3} = \frac{\text{OIP}_3}{\sqrt{2} \cdot S_{on,rms}} \tag{7.2}$$

where OIP_3 is an output-referred third-order intercept point and $S_{on,rms}$ is an output noise in RMS [62].

Table 7.5 summarizes a comparison of the filter characteristics and the relations between a supply voltage and an FOM are plotted in Fig. 7.22 for each filter. In Fig. 7.22 the lower a supply voltage and an FOM become, the more effective the filters are for a trade-off between supply voltage and dynamic range. While the reported filter in Ref. [16] can operate at the lowest supply voltage, the filter in Ref. [86] marks the best FOM in the recently published filters. In this circumstances, the proposed filter has achieved an FOM of 3.83 fJ from a 0.6-V supply voltage. As seen from the chart, the proposed technique in this thesis is effective for low-voltage and wide-dynamic range continuous-time filter design.

7.5   Conclusion

The measured results of two prototype filter chips are shown in this chapter. The one fabricated in a 0.35-μm CMOS technology has a 78-dB dynamic range from a power supply of 0.8 V. The filter uses the current-type SVC method and its effectiveness has been clarified from the measured results.

The another filter fabricated in a 0.18-μm CMOS technology achieves a 89-dB dynamic range from a 0.6-V supply voltage and an FOM of 3.83 fJ. The filter uses the

Table 7.5: Comparison to other recently published filters.

Author	V_{DD}	Power	order N [*1]	Technology	cutoff freq. f_c [*2]	In-band IIP_3	Output rms noise	Dynamic range DR_{OIP3} [*3]	FOM [*4]
Yoshizawa et al. [85]	2.7 V	11.6 mW	7	0.8μm BiCMOS	1.92 MHz	11 dBm	4.5 μV_{rms}	93 dB	1.84$\times$10^{-14} J
Guthrie et al. [86]	1.8 V	954 μW	10	0.18μm CMOS	3.27 MHz	20 dBV	444 μV_{rms}	106 dB	2.15$\times$10^{-16} J
Python et al. [39]	1.5 V	120 μW	2	0.35μm CMOS	45 kHz	6.54 dBμA	1.6 nA$_{rms}$	80 dB	1.26$\times$10^{-13} J
Giannini et al. [87]	1.2 V	21.6 mW	6	0.13μm CMOS	23.5 MHz	9.96 dBV	85 μV_{rms}	91 dB	4.14$\times$10^{-15} J
Notten et al. [88]	2.7 V	14 mW	10	0.25μm BiCMOS	9 MHz	136 dBμV	33 μV_{rms}	106 dB	8.06$\times$10^{-16} J
Elmala et al. [89]	1.4 V	13.5 mW	6	90nm CMOS	100 MHz	2 dBm	899 μV_{rms}	64 dB	1.52$\times$10^{-14} J
Krishnapura et al. [26]	2.5 V	26.1 mW	3	0.25μm BiCMOS	930 kHz	80 dBμA	4.4 nA$_{rms}$	127 dB	4.16$\times$10^{-15} J
Chatterjee et al. [16]	0.5 V	2.2 mW	5	0.18μm CMOS	135 kHz	-3 dBm	74 μV_{rms}	67 dB	1.52$\times$10^{-12} J
Ozgun et al. [54]	1.2 V	2.67 mW	5	0.18μm CMOS	100 kHz	-2.5 dBm	6.1 μV_{rms}	89 dB	1.94$\times$10^{-13} J
D'Amico et al. [90]	1.8 V	4.1 mW	4	0.18μm CMOS	10 MHz	17.5 dBm	16 μV_{rms}	97 dB	1.47$\times$10^{-15} J
Saari et al. [91]	1.2 V	24 mW	5	0.13μm CMOS	240 MHz	-35 dBm	527 μV_{rms}	30 dB	6.14$\times$10^{-13} J
Huang et al. [20]	1.0 V	1.6 mW	2	1.2μm CMOS	1.35 MHz	13.5 dBm	139 μV_{rms}	78 dB	7.81$\times$10^{-14} J
Palaskas et al. [62]	2.5 V	23 mW	10	0.25μm CMOS	19 MHz	17.4 dBm	15.6 μV_{rms}	101 dB	1.14$\times$10^{-15} J
Vasilopoulos et al. [21]	1.0 V	6.1 mW	5	0.12μm CMOS	10 MHz	20.1 dBm	267 μV_{rms}	79 dB	1.44$\times$10^{-14} J
This work	0.6 V	443 μW	5	0.18μm CMOS	100 kHz	42.5 dBμA	575 pA$_{rms}$	107 dB	3.83$\times$10^{-15} J

*1 If band-pass filters, N is the number of pole.

*2 If band-pass filters, its higher -3 dB edge is described.

*3 Calculated from Eq. (7.2).

*4 Calculated from Eq. (7.1).
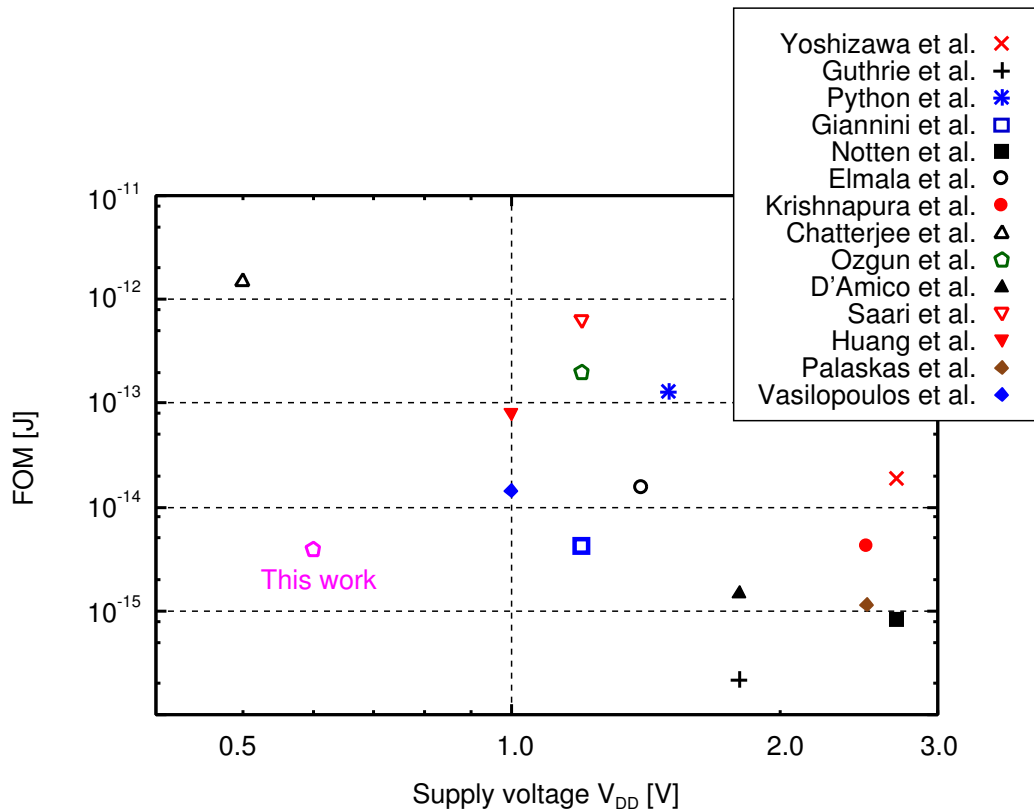
Figure 7.22: Comparison to other recently published filters: V_{DD} vs FOM.

voltage-type SVC method and also includes the voltage reference circuit generating 0.4 V from a 0.6-V supply and the automatic frequency tuning system, and thus has accomplished high integration because of no need of any external components. Furthermore the filter has been compared to other recently published filters in the viewpoint of a trade-off between a supply voltage and an FOM, and then has marked a good performance for the trade-off. From the comparison the effectiveness of the proposed techniques is confirmed.

Chapter 8

Conclusions

Design techniques of low-voltage wide-dynamic range CMOS log domain filters have been proposed. The filters were designed and implemented by use of the instantaneous and the syllabic companding techniques through Chapter 3 to 5. Furthermore low-voltage biasing circuits for the filters have been also presented in Chapter 6 to achieve high tolerance for a variation of supply voltage and temperature. Measured results of the filters have shown its effectiveness in comparison to conventional filters in Chapter 7.

The dissertation is summarized as follows. In Chapter 3 a synthesis method of all low-voltage instantaneous companding log domain integrators ware shown. The method clarified 45 integrators including four known topologies. Two 2nd-order Butterworth low-pass filters fabricated in a 0.35-μm CMOS technology as its application example were compared to each other through its measured results. Furthermore, a selection of a log domain integrator core from the generated integrators was also discussed for higher-order log domain filter design. In Chapter 4 a low-voltage syllabic companding technique was proposed by modifying the conventional dynamically adjustable biasing (DAB) technique. A control current dynamically adjusts appropriate operating points of DAB-based filters for low-voltage operation and wide-dynamic range. An externally linear and time invariant relation between an input and an output of filters was guaranteed by use of new two state variable correction methods. Simulation results showed that the proposed technique achieves wide-dynamic

range under low-supply voltage. Chapter 5 described an optimum design method of a control current in the view of dynamic range. The method uses a signal-to-noise-plus-distortion ratio as an evaluate function from an analyzed noise characteristic and a distortion model, which are a function of a control current and an input current amplitude. Since the method does not need any transient simulations, reducing the simulation time: reduction of about (5 minutes)/(240 minutes)=1/48. In Chapter 6 low-voltage biasing circuits, such as control current generators, a log-voltage reference circuit, and a frequency tuning system, were described. The control circuits include a low-voltage current peak detector and measured results of its prototype chip in a 0.35-μm CMOS process showed a wide-detection range from a 0.8-V supply. For low-voltage operation, the voltage reference circuit uses p-channel MOSFETs in weak inversion region instead of bipolar transistors in conventional bandgap reference circuits. The simulated results showed a temperature coefficient of -25.5 ppm/C$^\circ$ at 27 C$^\circ$. The fabricated reference circuit in a 0.18-μm CMOS technology outputs a stable 0.4 V from a power supply of 0.55 V at a room temperature. The frequency tuning system based on voltage-controlled filter was proposed by replacing a high-gain amplifier with a duty ratio detector and a charge pump circuit for low-voltage operation. Stability analysis of the system was also described. These biasing circuits are applicable to any low-voltage log domain filters. Measured results of two prototype 5$^{\text{th}}$-order Chebychev low-pass filters were shown in Chapter 7. The one was fabricated in a 0.35-μm CMOS technology and the another was done in a 0.18-μm CMOS. The former achieves 78-dB dynamic range at a power supply of 0.8 V. On the other hand the latter filter has a dynamic range of 89 dB and consumes 443 μW, and was compared to other recently published filters through a figure of merit (FOM) which is calculated by use of dynamic range, bandwidth, filter order, and power consumption. The FOM is 3.83 fJ at a power supply of 0.6 V and thus the filter has marked an effective performance in the view of a trade-off between a supply voltage and dynamic range.

Future works are as follows:

Optimum design of log domain filter cores: Although an optimum design method of a control current has been described in Chapter 5, parameters of a log domain filter core, such as capacitances and transconductances, must be also considered for a truly optimum design of syllabic companding log domain filters. Since a log domain filter core decides a noise and a distortion performance as well as a control current, an appropriate decision of the parameters must be undertaken before an optimum design of the control current described in Chapter 5. Some arrangements for conventional optimum design methods of G_m-C filters would be needed because a log domain filter core is a non-linear circuit.

Tolerance for process variation: The proposed low-voltage filters use MOSFETs in subthreshold and thus a drain current is expressed as an exponential function of a gate-to-source voltage. Therefore, if a variation of threshold voltage exists, an error of drain current arises exponentially, which leads to large relative errors for filter characteristics compared to circuits with strong inversion MOSFETs. Since it is said that a variance of threshold voltage is inversely proportional to the square root of the product of channel length and width, a large aspect ratio for MOSFETs is used in the proposed filters. Nevertheless, an influence of filter characteristics from the variation must be analyzed and discussed.

Blocker immunity: Syllabic companding filter is a dynamic circuit, which dynamically changes its characteristic. In the proposed filters a control current is determined to be proportional to an input or an output current envelope, appropriately amplifying the internal voltage swings at an input stage of the filter for wide-dynamic range. However, if a blocker, or an out-of-band signal, is larger than a desired in-band signal, a signal-to-noise ratio of the filter degrades because an appropriate control current for the desired signal is not applied to the filter anymore when an envelope is obtained from the filter input. On the other hand if an envelope is sensed from the output in the same situation, then a distortion arises at the input stage of the filter. This fact is also observed from measured results of out-of-band third-order input-referred intercept point (IIP$_3$) in Chapter 7: out-of-band IIP$_3$'s are

smaller than in-band ones.

Common-mode noise suppression: Since log domain circuits are internally non-linear one for the input and the output, common-mode noise from the substrate of silicon and clocked line due to capacitor coupling is not able to suppress at the output in theory. If one wants proactively to integrate such the log domain circuits with digital circuits on the same chip, a method of common-mode noise suppression must be considered.

Applying to practical applications: The prototype chips of the proposed filters occupy more than 2 mm^2, especially capacitors are a most dominant. Therefore reduction of active area would be needed in practical applications for low-cost products. Furthermore, if a wireless application is assumed, one might design a syllabic companding log domain complex filter to process quadrature signals.

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Appendix A

Log Domain Filter Synthesis and State Variable Correction

A.1   Synthesis of All-Pole Log Domain Filters

A.1.1   Synthesis

An all-pole higher-order low-pass filter is synthesized by use of an RLC proto-type ladder shown in Fig. A.1 (a), which is a 3rd-order low-pass filter as an example. In Fig. A.1 (a) KVL and KCL give equations as follows:

$$
\begin{aligned}
sC_1 V_1 &= \frac{1}{R}(V_{in} - V_1) - I_2 \\
sL_2 I_2 &= V_1 - V_{out} \\
sC_2 V_{out} &= I_2 - \frac{1}{R}V_{out}.
\end{aligned}
$$

These equations are transformed by introducing $V_2 = RI_2$ into

$$
\begin{aligned}
V_1 &= \frac{V_{in} - V_1 - V_2}{sC_1 R} \\
V_2 &= \frac{V_1 - V_{out}}{sL_2/R} \\
V_{out} &= \frac{V_2 - V_{out}}{sC_3 R}
\end{aligned}
$$

where $1/\Omega_1 = RC_1$, $1/\Omega_2 = L_2/R$, and $1/\Omega_3 = RC_3$. Therefore the RLC ladder filter shown in A.1 in redrawn as a configuration using integrators Ω_1/s, Ω_2/s, and Ω_3/s, a signal flow graph (SFG) of which is shown in Fig. A.1 (b). In Fig. A.1 (b) an output of
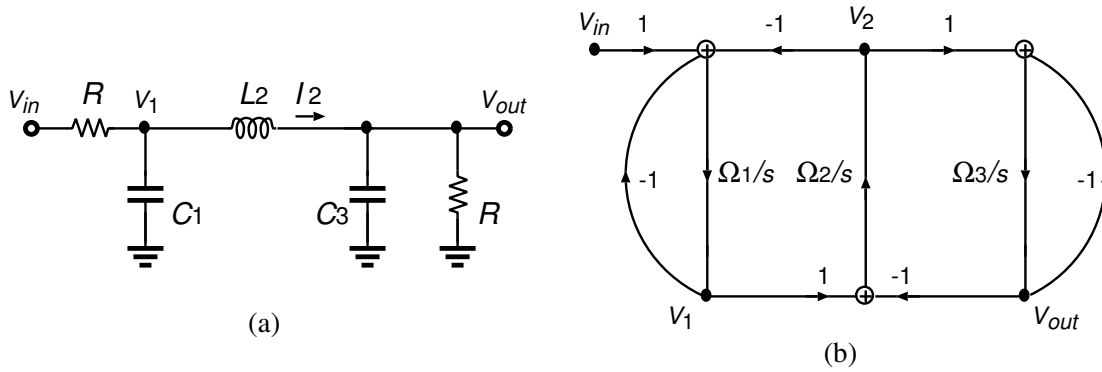
Figure A.1: All-pole filter synthesis using Leap-frog simulation (3rd-order low-pass filter as an example). (a) RLC prototype ladder and (b) signal flow graph (SFG) of (a).

an integrator is connected to an input of other integrators. In other words integrators are cascaded each other. The upper side figure of Fig. A.2 shows a situation of the cascaded connections when a log domain integrator is used as an integrator. As seen from Fig. A.2 since an expander M_{out} of the former integrator and a compressor M_{in} of the latter one have a relation of a reciprocal function each other, these MOSFETs are canceled out and the log domain integrator cores are directly cascaded. Therefore all-pole higher-order log-domain filter core, which is a part of a log domain filter, can be synthesized by use of log domain integrator cores [39], [46].

A.1.2 State Variable Correction for Applying to Syllabic Companding Technique

When the syllabic companding technique is applied to a higher-order log domain filter described above, a state variable correction (SVC) is required for a log domain filter core because of an ELTI relation. In Chapter 4 it is shown that there are two SVC methods: a current-type and a voltage-type SVC methods, and log domain integrator cores with these SVCs are shown in Fig. A.3. Since a higher-order log domain filter core is synthesized by using log domain integrator cores, the log domain filter cores on syllabic companding filter is also designed by using integrator cores with SVCs.
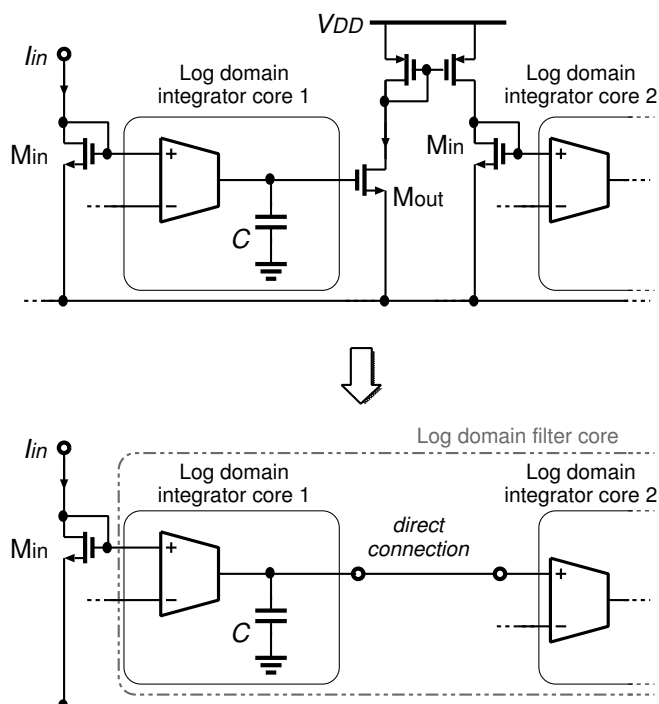
Figure A.2: Principle of all-pole higher-order filters based on log domain integrators [39], [46].
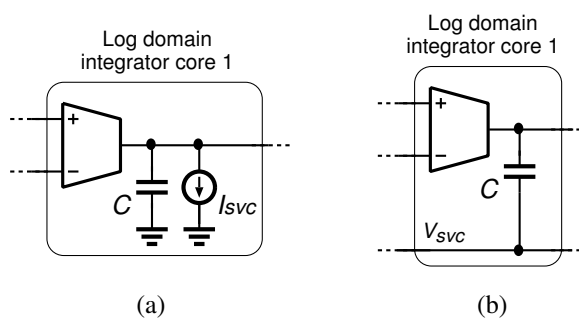

Figure A.3: Log domain integrator cores in all-pole syllabic companding log domain filters using (a) current-type SVC and (b) voltage-type SVC.

A.2   Synthesis of Log Domain Filters with Transmission Zeros

A.2.1   Synthesis

Figure A.4 (a) shows an RLC prototype ladder filter of a $3^{\rm rd}$-order low-pass filter with transmission zeros. Zeros are realized due to a capacitor C_2 and makes a

precipitous roll-off. In Fig. A.4 (a) KVL and KCL lead to equations as

$$sC_1V_1 = \frac{1}{R}(V_{in} - V_1) - sC_2(V_1 - V_{out}) - I_2$$

$$sL_2I_2 = V_1 - V_{out}$$

$$sC_3V_{out} = sC_2(V_1 - V_{out}) + I_2 - \frac{V_{out}}{R}$$

and assuming a nodal voltage $V_2 = RI_2$,

$$V_1 = \frac{V_{in} - V_1 - V_2}{s(C_1 + C_2)R} + k_1 V_{out}$$

$$V_2 = \frac{V_1 - V_{out}}{sL_2/R}$$

$$V_{out} = \frac{V_2 - V_{out}}{s(C_2 + C_3)R} + k_3 V_1$$

are obtained where $k_1 = C_2/(C_1 + C_2)$, $k_3 = C_2/(C_3 + C_2)$, $1/\Omega_1 = R(C_1 + C_2)$, $1/\Omega_2 = L_2/R$, and $1/\Omega_3 = R(C_3 + C_2)$. Therefore an equivalent ladder filter is shown in Fig. A.4 (b) and its SFG is done in Fig. A.4 (c). This means that a log domain filter with transmission zeros is composed of integrators and summing circuits.

Next, a log domain filter is designed by transforming the SFG shown in Fig. A.4 (c) into a log domain SFG [71]. If blocks "L" and "E" which mean a logarithmic compressor and an exponential expander expressed as

$$\hat{V}_i = nU_T \ln\left(\frac{I_i + I_g}{I_g}\right) + V_b \tag{A.1}$$

$$I_o = I_g \exp\left(\frac{\hat{V}_o - V_b}{nU_T}\right), \tag{A.2}$$

respectively, are introduced and are adjacently inserted into each brunch of the SFG shown in Fig. A.4 (c), then a log domain SFG as shown in Fig. A.4 (d) is obtained. In Fig. A.4 (d) a transfer function between the two SFGs is equal because Eqs. (A.1) and (A.2) are reciprocal functions except for a bias current I_g. Parts surrounded by dashed line corresponds to a log domain integrator core described in Chapter 4 and parts surrounded by dashed-dotted line is a log domain summing circuit shown in Fig. A.5 [92], which is required unlike an all-pole filter design. The summing circuit
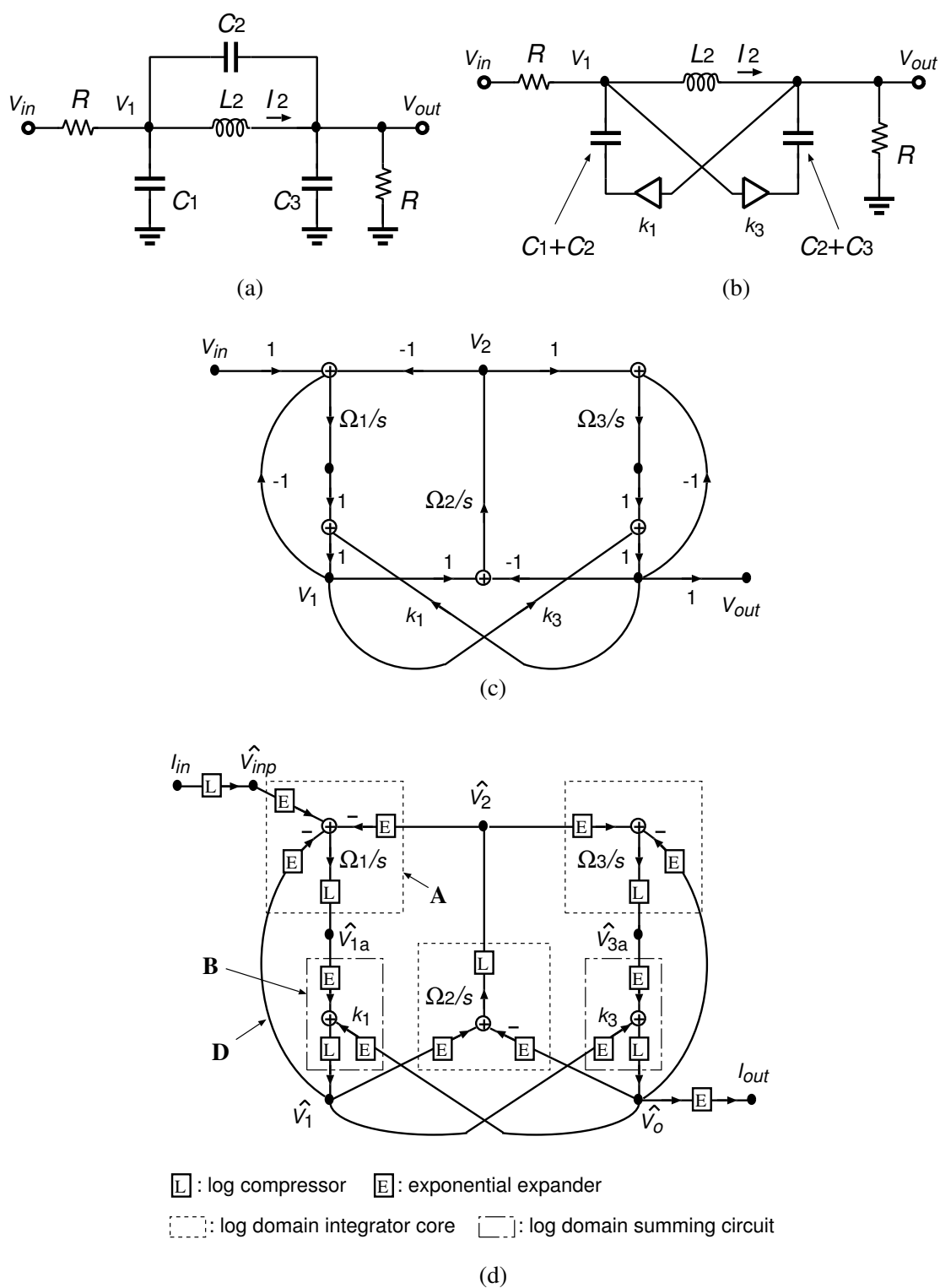
Figure A.4: Log domain filter synthesis using Leap-frog simulation (3$^{\mathrm{rd}}$-order low-pass filter as an example). (a) RLC prototype ladder, (b) equivalent circuit of (a), (c) signal flow graph (SFG) of (a), and (d) log domain SFG [71].
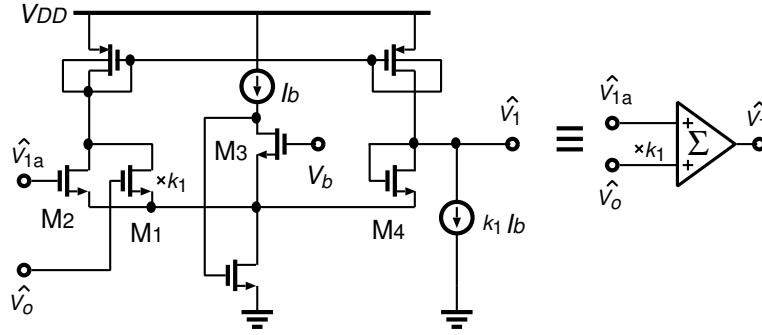
Figure A.5: Log domain summing circuit.

shown in Fig. A.5 has a characteristic expressed as

$$I_b \exp\left(\frac{\hat{V}_1 - V_b}{nU_T}\right) = I_b \exp\left(\frac{\hat{V}_{1a} - V_b}{nU_T}\right) + k_1 I_b \exp\left(\frac{\hat{V}_o - V_b}{nU_T}\right) - k_1 I_b \qquad (A.3)$$

where an aspect ratio of M_1 is determined by separating the size from that of M_2 to M_4 with a coefficient $k_1 = C_2/(C_1 + C_2)$. Conclusively a log domain filter core with transmission zeros is designed by using log domain integrator cores and log domain summing circuits.

A.2.2 State Variable Correction for Applying to Syllabic Companding Filters

When syllabic companding technique is applied to a log domain filter with transmission zeros, a current I_g becomes time-variant $I_g(t)$ and thus SVC is required. In this section, required signals for SVC are derived by using a part of a log domain filter core shown in Fig. A.4 (d). If an integrator core labeled as **A** and a summing circuit as **B** except for a feedback path as **D** in Fig. A.4 (d) are only considered, a partially circuit of the filter core is expressed as in Fig. A.6. Figure A.6 (a) shows a circuit with current-type SVC using a current I_{SVC} and (b) does one with voltage-type SVC using a voltage V_{SVC}. In Fig. A.6 (a) if a compressor expressed as Eq. (A.1) is connected to the nodes $\hat{V}_{in}$, $\hat{V}_2$, and $\hat{V}_o$ and an expander as Eq. (A.2) is also done to $\hat{V}_1$ and a required SVC current I_{SVC} is applied, then an expected differential
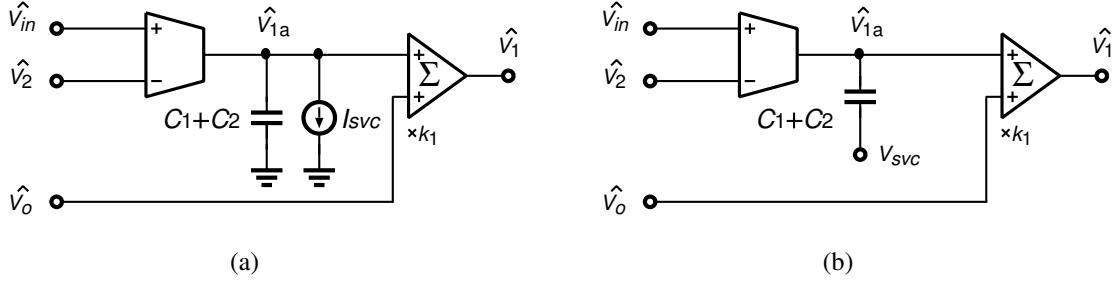
Figure A.6: Log domain integrator core and log domain summing circuit in syllabic companding filter with transmission zero.

equation in current domain becomes

$$\Omega_1(I_{in} - I_2) + k_1\frac{dI_{out}}{dt} = \frac{dI_1}{dt} \tag{A.4}$$

where subscripts of all the current names correspond to that of the voltage ones. KCL at the top terminal of the capacitor in Fig. A.6 (a) gives as

$$(C_1 + C_2)\frac{d\hat{V}_{1a}}{dt} + I_{SVC} = I_0\left[\exp\left(\frac{\hat{V}_{in} - \hat{V}_{1a}}{nU_T}\right) - \exp\left(\frac{\hat{V}_2 - \hat{V}_{1a}}{nU_T}\right)\right]. \tag{A.5}$$

Substituting Eq. (A.1), a reciprocal function of Eq. (A.2), and a function derived for $\hat{V}_{1a}$ at Eq. (A.3) into Eq. (A.5) and comparing to Eq. (A.4), then a required SVC current I_{SVC} for an ELTI relation of the circuit shown in A.6 (a) is obtained as

$$I_{SVC} = nU_T(C_1 + C_2)\frac{dI_g}{dt}\frac{1}{I_g} \tag{A.6}$$

where a unity gain angular frequency Ω_1 is equals to $I_0/\{nU_T(C_1 + C_2)\}$. Since the SVC current I_{SVC} is the same as Eq. (4.11), the current is generated by use of an SVC circuit shown in Fig. 4.4.

Another SVC is to control the bottom terminal of the capacitor by V_{SVC} as shown in Fig. A.6 (b) and thus KCL at $\hat{V}_{1a}$ leads to

$$(C_1 + C_2)\frac{d(\hat{V}_{1a} - V_{SVC})}{dt} = I_0\left[\exp\left(\frac{\hat{V}_{in} - \hat{V}_{1a}}{nU_T}\right) - \exp\left(\frac{\hat{V}_2 - \hat{V}_{1a}}{nU_T}\right)\right]. \tag{A.7}$$

The same derivation of the equation as the above gives

$$V_{SVC} = nU_T\ln\left(\frac{I_S}{I_g}\right) + V_b \tag{A.8}$$

which is the same as Eq. (4.13). Therefore a connection shown in Fig. 4.5 is also available for higher-order syllabic companding log domain filter cores with transmission zeros.