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Development of an Evaluation Platform and Performance Experimentation of Flex Power FPGA Device

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SUMMARY Field-programmable gate array (FPGA) devices are applied for accelerating specific calculations and reducing power consumption in a wide range of areas. One of the challenges associated with FPGAs is reducing static power for enforcing their power effectiveness. We propose a method involving fine-grained reconfiguration of body biases of logic and net resources to reduce the static power of FPGA devices. In addition, we develop an FPGA device called Flex Power FPGA with SOTB technology and demonstrate its power reduction function with a 32-bit counter circuit. In this paper, we describe the construction of an experimental platform to precisely evaluate power consumption and the maximum operating frequency of the device under various operating voltages and body biases with various practical circuits. Using the abovementioned platform, we evaluate the Flex Power FPGA chip at operating voltages of 0.5–1.0 V and at body biases of 0.0–0.5 V. In the evaluation, we use a 32-bit adder, 16-bit multiplier, and an SBOX circuit for AES cryptography. We operate the chip virtually with uniformed body bias voltage to drive all of the logic resources with the same threshold voltage. We demonstrate the advantage of the Flex Power FPGA by comparing its performance with non-reconfigurable biasing.

key words: *FPGA, programmable body biasing, evaluation platform, static power consumption*

1. Introduction

Field programmable gate array (FPGA) devices have been employed for specific processing and prototyping. Increasingly, FPGAs are being used for server acceleration, network traffic processing, machine learning, sensor preprocessing, and control functions. In the Internet of Things/Everything (IoT/IoE) era, more effective processing and lower power operation are needed for the application of FPGAs as edge devices.

To this end, we propose a method for reducing the static power of FPGA devices by means of fine-grained reconfiguring of the body biases of logic and net resources. Additionally, we develop an FPGA chip called Flex Power FPGA by using silicon-on-thin buried oxide (SOTB) technology to operate at low voltages. In preliminary evaluations, we estimated the effectiveness of our method by simulation [1] and confirmed the chip functions of body biasing and low-voltage operation by using a 32-bit counter circuit [2].

To evaluate the performance with a practical circuit and to explore further improvements, we must verify its opera-

tion precisely and measure its power consumption and maximum frequency automatically based on a number of parameters. In addition, a synthesis tool is needed to implement sophisticated circuits and to support multiple sources. For these reasons, we constructed an experimental platform for evaluating and verifying the Flex Power FPGA chip. The platform was designed to be expandable for future and other devices. Using this platform, we experimented with a 16-bit multiplier, a 32-bit adder, and four SBOX blocks of AES [11] circuits. In the experimentation, we compared the reconfigurable biasing with unified biasing for the whole device to demonstrate the efficiency of our method.

2. Flex Power FPGA

The purpose of our method is to reduce static power without affecting performance and to increase the operating frequency of the device at low voltages.

The power consumption of a device is the sum of its dynamic power and its static power. Dynamic power is mainly from switching current, which is proportional to parasitic capacitance, switching counts, and the square of the operating voltage. Driving a device at lower voltages is effective for reducing dynamic power. Static power results from leakage current, which depends on the process, temperature, and the subthreshold current related to the threshold voltage. The subthreshold current can be reduced by increasing the threshold voltage; however, this approach leads to an increase in delay [3].

Since a device that has a concrete function can be designed based on the trade-off between performance and power consumption, it is difficult to select an appropriate tradeoff for the FPGA. An FPGA consists of redundant circuit elements, which facilitate a myriad of circuit implementations. Thus, designers cannot predict the performance tradeoff. Additionally, a large number of elements are unused in general circuits, but their locations change extensively and are unpredictable.

To reduce static power and to improve FPGA performance at low operating voltages, we propose a dedicated method for FPGAs that is based on fine-grained threshold voltage control. Figure 1 shows the concept of our method. According to the implemented circuits, a low threshold voltage is set in the logic element in the critical path to drive fast, whereas the static power consumed by the unused elements and the slower paths is reduced. We choose fine-grained voltage control so that the voltages of all of the FPGA el-

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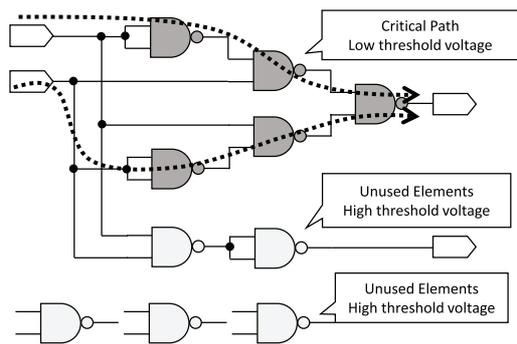


Fig. 1 Concept of proposed method.

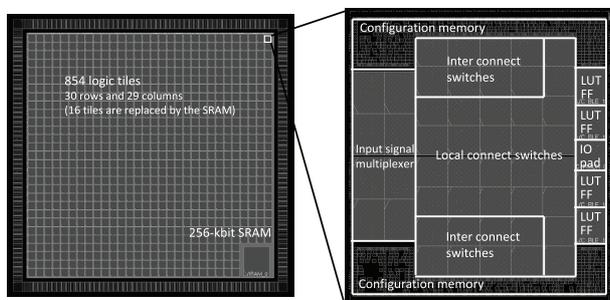


Fig. 2 Photo of the Flex Power FPGA chip.

Table 1 Power supply ports of the FPGA chip.

VCORE	Core logic
VMEM	Configuration memory and 256-kb SRAM
VHVMH	Body bias control power
VHVML	Body bias control power
VBPH	Bias voltage of PMOS for low power
VBNH	Bias voltage of NMOS for low power
VBPL	Bias voltage of PMOS for high performance
VBNL	Bias voltage of NMOS for high performance
VDDL	Level shifter of I/O from core voltage to 1.2 V
VDDH	Level shifter of I/O from 1.2 V to 3.3 V
VCCQ	I/O
VSS	GND

elements, look-up tables (LUTs), flip-flops (FFs), and interconnect switches can be controlled individually.

2.1 Details of the Device

The chip of the Flex Power FPGA device was fabricated using 65-nm SOTB technology [4]. A photo of the chip is shown in Fig. 2. 854 logic tiles were included, and each tile comprises four LUT-FF pairs (BLE, basic logic element). The total amount of logic resources is 3416 BLEs. Each tile has 16 interconnect switch boxes (SMUX), 24 local connect switches (LMUX), 8 input signal multiplexers (IMUX), and an IO pad. There is 256-kbit of SRAM on the chip.

The chip requires 11 power supplies for experimentation (Table 1). V_{CORE} is for logic elements, and it is affected by the threshold voltage. VHVMH, VHVML, VBPH, VBNH, VBPL, and VBNL are power supplies for biasing.

Figure 3 shows the reconfigurable threshold voltage

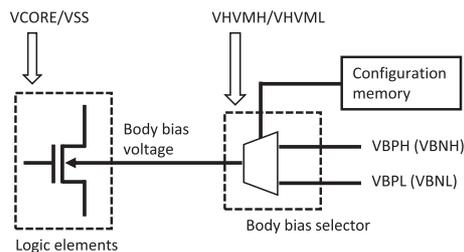


Fig. 3 Reconfigurable threshold voltage block.

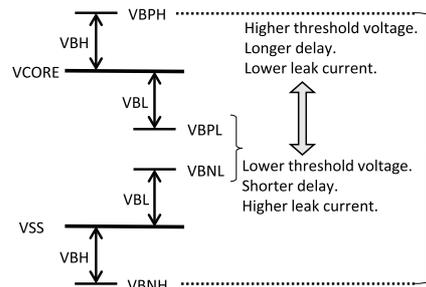


Fig. 4 Relationship among bias voltages.

block. There are two pairs of body bias voltages, and they are switched by a bias selector circuit according to the configuration memory. SOTB technology offers wide controllability of the threshold voltage by means of body biasing [4]. By employing the characteristics of SOTB, static current and delay of the logic gates can be controlled by changing the body bias voltage.

Generally, the VBPH-VBNH pair is used to set a high threshold voltage for suppressing static power. By contrast, the VBPL-VBNL pair is used for increasing drive speed. The body bias voltage of the p-mos and the n-mos are set using the following expression.

$$VBPH = V_{CORE} + VBH$$

$$VBNH = GND - VBH \quad (VBH > 0)$$

$$VBPL = V_{CORE} - VBL$$

$$VBNL = GND + VBL \quad (VBL > 0)$$

Figure 4 shows the relationship among the bias voltages. Control voltage VHVMH and VHVML are driven by the same voltage as VBPH and VBNL. The gate-level architecture of the bias selector is shown in [5].

To focus on the effectiveness of the threshold voltage to V_{core} power consumption, body biasing is not applied to the configuration logic and memory, level shifter, or I/O block.

2.2 Device Evaluation

In previous work, manual experimentation was conducted using a 32-bit counter circuit, where the count status was presented to an outer LED indicator and a logic analyzer. To evaluate and improve the Flex Power FPGA chip, we must verify its circuit and measure its power consumption

with several VCORE, VBH, and VBL voltages, and operational frequency parameters with varied circuits. It is difficult to conduct manual experimentation owing to complications such as supplying power from 11 sources, applying clock frequency, validating circuit operation, finding the maximum operating frequency, and configuring the circuit. To support further evaluation, we designed an evaluation platform that performs verification automatically and improves test reproducibility. To evaluate the effectivity of future improvements, the platform is designed to be capable of testing other devices for comparison under the same conditions.

3. Evaluation Platform

The developed evaluation platform includes an automatic testing environment and a circuit synthesis tool chain.

Figure 5 shows the architecture of the testing environment. It consists of a fixture board for the Flex Power FPGA chip, a control FPGA board, source measurement units (SMUs), a function generator, and a host PC. The SMUs are three Keysight U2722A and a Keysight B2962A; they supply and measure 11 power sources. Control and collection of measured data are performed through USB by the host PC. The function generator and the control FPGA board are also operated through USB. The structure of software on the host PC is shown in Fig. 6. The testing is mainly controlled by the TestProcedure class as shown in Fig. 7. Device-specified functions, such as configuration and control pro-

ocols, and control protocols of instruments are transparent to the testing procedure class. VISA-supported instruments and other device can be added by preparing a class that denotes specific commands and functions in C# language. The pseudo power supply can be constructed with other combi-

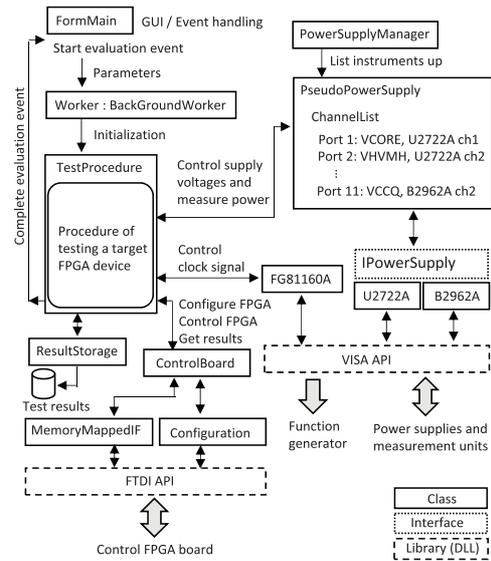


Fig. 6 Structure of the testing software.

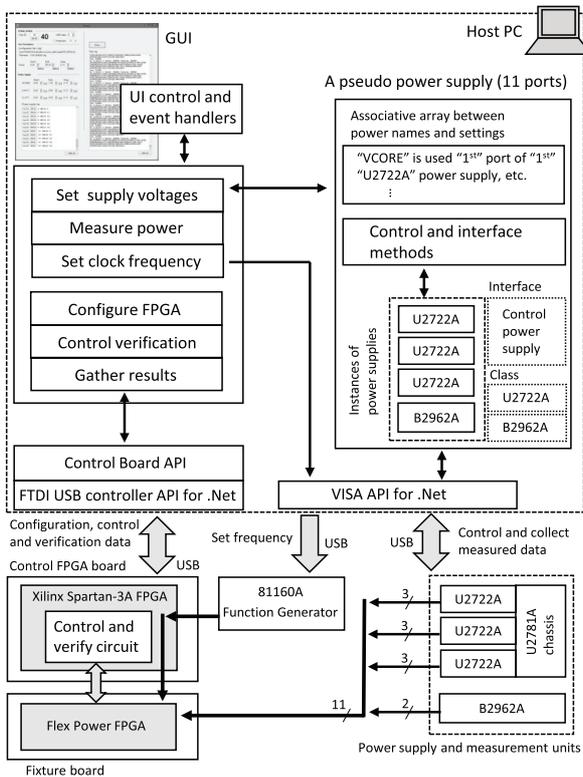


Fig. 5 Architecture of the testing environment.

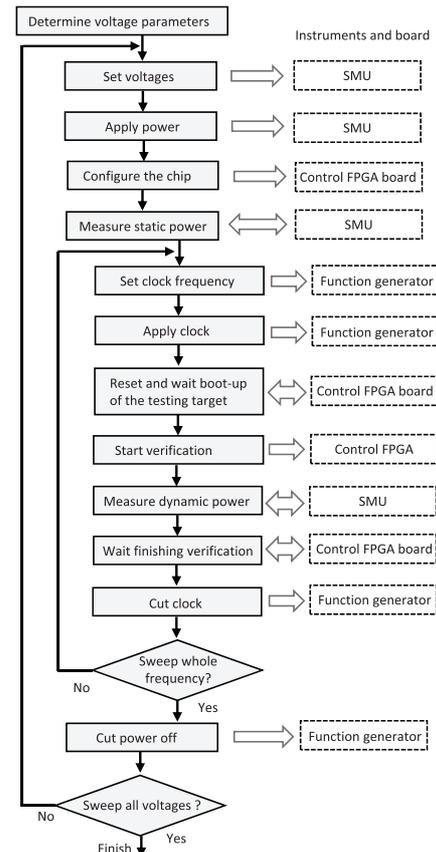


Fig. 7 Testing procedure of the environment.

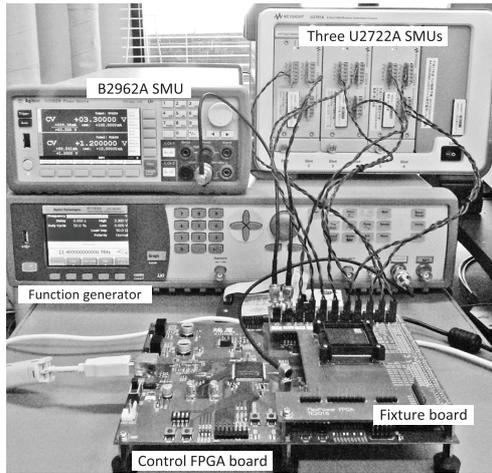


Fig. 8 The setup of the testing environment.

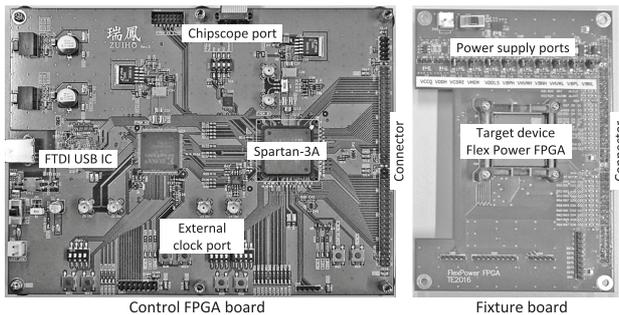


Fig. 9 The control board and the fixture board.

nations of power supplies according to power requirement of the target device. The setup of the testing environment in this paper is shown in Fig. 8.

In a typical test configuration, the target Flex Power FPGA chip is placed on the fixture board mounted on the control board. A picture and the main components of the boards are shown in Fig. 9. The control board is equipped with a Xilinx Spartan-3A 3400DSP FPGA, an interface connector, a USB controller, and a Xilinx chipscope debugging port. The control and the fixture board are connected by 32-bit data, 4-bit status, reset, and clock signals. The text fixture board is mainly equipped with a socket for a target chip, power supply ports, and an interface connector. It is designed simply to ease development of an alternate fixture board based on the original one for supporting other devices.

The Spartan-3A FPGA is implemented as a circuit that includes a control block with a fixed 24 MHz clock and a verification block with a flexible clock. A block diagram of the circuit is shown in Fig. 10. The control block consists of a channel to communicate with the host PC, testing controller, and configuration of the Flex Power FPGA. The verification block consists of a reference module, testing functions, and a Xilinx chipscope internal logic analyzer. The reference module is checked in advance via simulation at the maximum clock frequency, and an equivalent module is

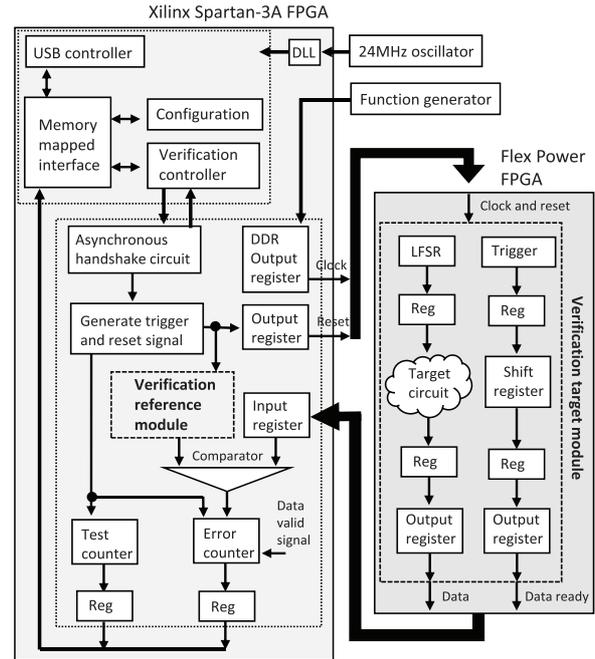


Fig. 10 Block diagram of the verification circuit.

implemented as a target module to the Flex Power FPGA[†]. The testing circuit verifies the output of the internal reference circuit and the Flex Power FPGA one million times and counts the number of cycles with mismatched data.

The verification target module circuit for the Flex Power FPGA comprises a data processing block and a data-ready signal generator. The data processing block has a target circuit and an LFSR counter that generates test vectors. The ready signal block generates valid data and trigger signals. Registers are placed to suppress fan-out signal delay and delay from data to the output pad.

The target circuit is operated continuously by the LFSR test vector in the verification period to measure dynamic power consumption. This is because in general, SMUs do not measure timing in high accuracy^{††}. While circuit verification is terminated at one million cycles, circuit operation is continued until the measurement is complete.

We improved our synthesis tool chain [6] to support multiple modules, fixed values, and Verilog-HDL source files for facilitating the implementation of practical circuits. We employed yosys [7] and ABC [8] tools, and added pre-processing and post-processing to the module description file and the LUT mapping information. A block diagram of the tool chain is shown in Fig. 11. A GUI-based development environment was designed using the .Net Framework to ensure that the synthesis flow was transparent. The configuration data was generated from Verilog HDL files and pin assignment file.

[†]It is supposed that Spartan-3A FPGA is faster than Flex Power FPGA. The circuit is implemented with a timing constraint at 75 MHz clock operation.

^{††}In general, the accuracy of SMUs is around 10 μ s.

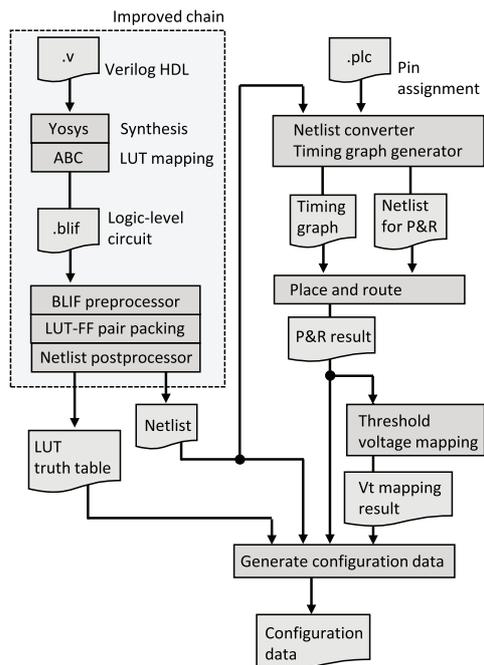


Fig. 11 Block diagram of the synthesis tool chain.

4. Experimentation

We conducted experimentation on the Flex power FPGA with three practical circuits, and evaluated the static power, operating frequency and dynamic power. To evaluate the effectiveness of the fine-grained biasing (Flex Power), we compared the Flex Power with uniformed body bias (Unified biasing), wherein the chip was operated virtually and the same bias voltage was applied to the entire chip. The implemented circuits were a 32-bit adder (ADD32), a 16-bit multiplier (MUL16), and four AES-SBOX (SBOX). The 16-bit multiplier and the 32-bit adder consisted of ripple carry adders to emphasize the difference between the critical path and other elements. The AES-SBOX was constructed by employing normal basis representation of the Galois field $GF(2^{2k})$ [12].

4.1 Experimental Conditions

The operational core voltage of the chip was 0.5–1.0 V, and the range of VBH and VBL was 0.0–0.5 V. The experimental range of the operating frequency was extracted by testing preliminarily the best and the worst cases of the threshold voltage. Power consumption was measured eight times and averaged for each frequency.

The resource usage of the circuits is shown in Table 2. In the table, “(LVT)” denotes the number of resources that was applied a forward bias voltage. The result shows that the number of LVT elements is a small ratio. In other words, only a few logic elements should be operated fast.

Table 2 Occupied resources of circuits.

	ADD32	MUL16	SBOX
LUT	175	766	316
FF	197	133	133
BLE	275	834	386
BLE (LVT)	8	17	16
IMUX (LVT)	80	800	369
SMUX (LVT)	369	1721	671
LMUX (LVT)	8	22	20

4.2 Static Power and Frequency with Back-Biasing

The static power and the maximum operating frequency of Flex Power and unified biasing with back-biasing are shown in Figs. A·1–A·12. In this evaluation, VBL was fixed at 0.0 V. In the graph, the left-side bar of each voltage shows the power when bias voltage is not applied. The bars shows the power when VBH is 0.0 V, 0.1 V, 0.2 V, 0.3 V, 0.4 V, and 0.5V.

The graph of power consumption shows that the static power levels of Flex Power and unified biasing are approximately the same for all of the circuits. The power of the bias circuit (VBIAS) increases at an exponential rate independently of the biasing and the circuits. This tendency of VBIAS had already been discovered in a previous evaluation using a 32-bit counter [5].

By contrast, the graphs of maximum frequency present significant differences. While the frequency drops proportionally with unified biasing, the drop when using Flex Power is 2 MHz in the worst case. The tendency is presented for each circuit in spite of the different ranges of operating frequency. This results demonstrate that Flex Power decreases static power with a slight delay, and most of the results show that back-biasing voltages of 0.2 V and 0.3 V are the most suitable.

4.3 Static Power and Frequency with Forward-Biasing

The power and frequency results with forward-biasing are shown in Figs. A·13–A·24. In this evaluation, VBH was fixed at 0.0 V. In the graph, the left-side bar of each voltage shows the power when no bias voltage is applied.

It is clear that the operational frequency is boosted by forward-biasing, and the power efficiency of the Flex Power provides a significant advantage[†]. It is noteworthy that the power consumption of the core increases by different amounts in spite of the condition that the ratio of the critical-path resources is constant at around 5%. By contrast, VBIAS does not change. We estimate the reason for this is that the range of the biasing control voltage is within V_{CORE} to V_{SS}.

4.4 Dynamic Power

The dynamic power levels are shown in Figs. 12–14. In

[†]Note that the y-axes of these graphs are different between Flex Power and unified biasing.

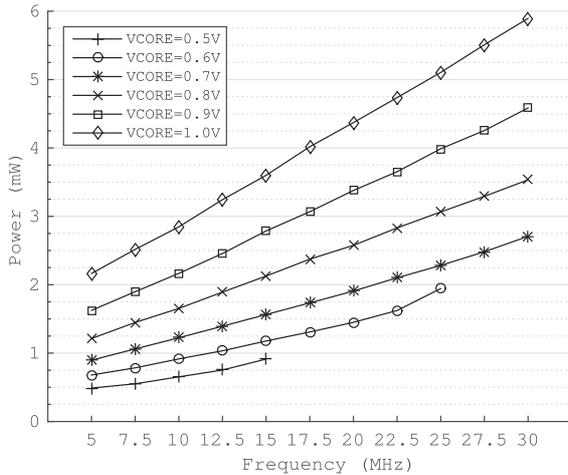


Fig. 12 Dynamic power of the ADD32 circuit.

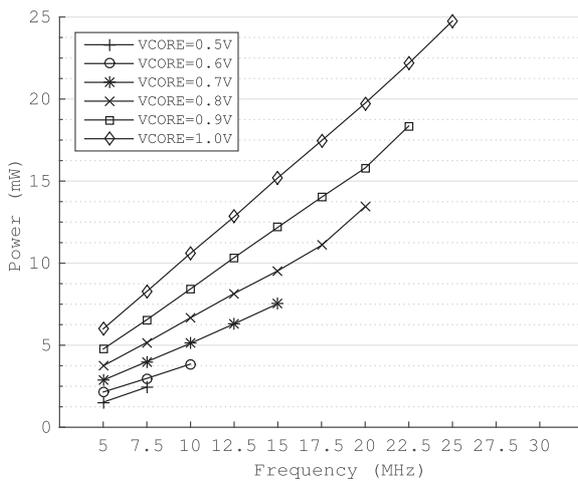


Fig. 13 Dynamic power of the MUL16 circuit.

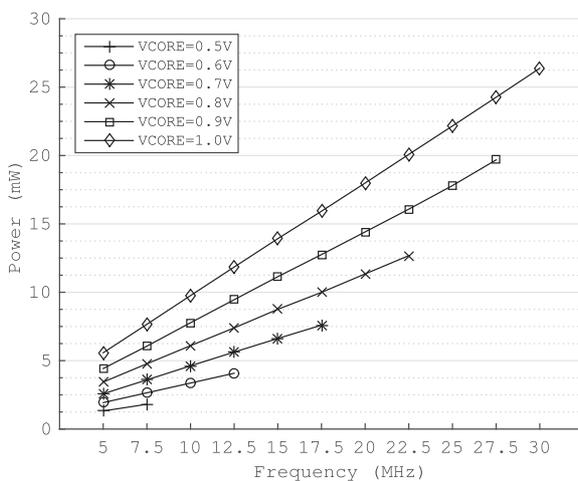


Fig. 14 Dynamic power of the SBOX circuit.

this graph, the lowest power consumption at each frequency is plotted. Therefore, the combinations of VBH and VBL are independent. The dynamic power consumption levels are considerably higher than the static power consumption

levels because the target circuit operates continuously with pseudo-randomized data.

The result demonstrates that the Flex Power FPGA has the advantage of variable application by employing the core and biasing voltages as the operational frequencies of the circuits and of delivering the demanded processing performance. For example, consider the case in which the maximum frequency of MUL16 is 16 MHz at the core voltage of 0.8 V without biasing (see Fig. A-19). Then, the operational frequency can be boosted to 20 MHz by forward-biasing, and the power consumption is lower in comparison to that at the core voltage of 0.9 V.

4.5 Considerations

In this paper, we demonstrate the advantage of our method in terms of static power consumption and adaptability by using three circuits. More variations of the target circuits, such as a circuit that occupies most of the logic resources, are required to explore additional points of improvement.

The testing environment was designed to accommodate both the Flex Power FPGA and future devices. It is expandable to support other chips; however, the maximum testing frequency is limited by the control FPGA of the reference module and the local bus width can be extended up to 64-bit.

To investigate the energy efficiency, a current and voltage measurement system with a sampling rate greater than 100 MHz is required to measure power consumption in each clock cycle. High-rate sampling is needed to observe the power in the active and the inactive conditions of the target circuits. For example, the Keysight CX3300 series of precise current measurement systems is one such choice.

5. Conclusion

In this paper, we developed an evaluation platform to verify our FPGA devices with practical circuits. The platform was designed to support future and other FPGA devices for further comparison experiments. We also evaluated the 65-nm Flex Power FPGA STOB chip with fine-grained reconfigurable body biasing in terms of static power, operating frequency, and dynamic power. We operated virtually the chip with uniformed body bias voltage in order to drive the logic resources with same threshold voltage.

We evaluated the efficiency of the Flex Power FPGA in comparison with unified biasing. The experimental result demonstrated the advantage of our method in terms of static power and adaptability with a 32-bit adder, a 16-bit multiplier, and of AES SBOX circuits.

In future work, we plan to implement DES and AES cryptographic circuits as testing targets that use large logic resources.

Acknowledgments

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Appendix

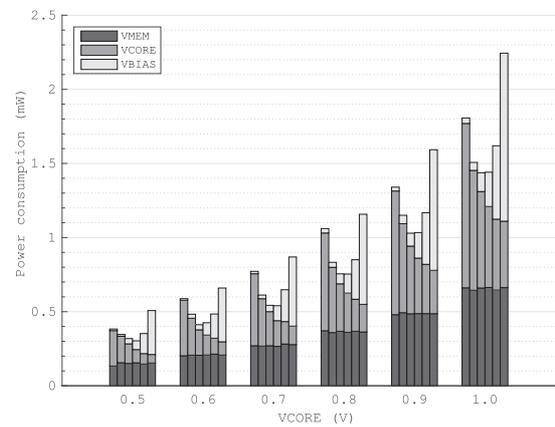


Fig. A-1 Static power of the ADD32 circuit with Flex Power.

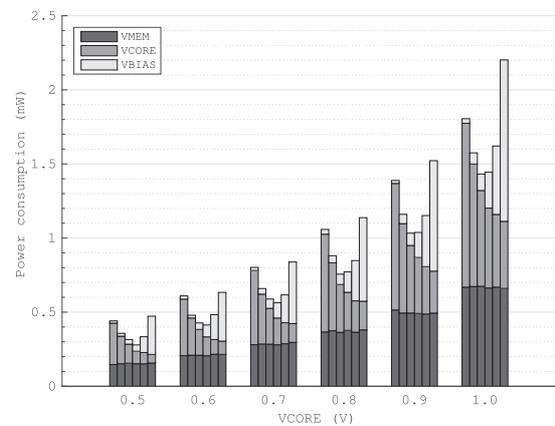


Fig. A-2 Static power of the ADD32 circuit with unified biasing.

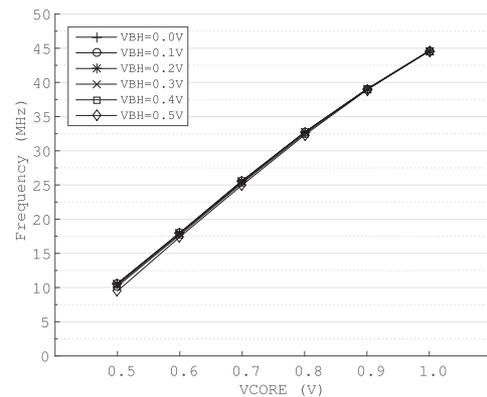


Fig. A-3 Max frequency of the ADD32 circuit with Flex Power.

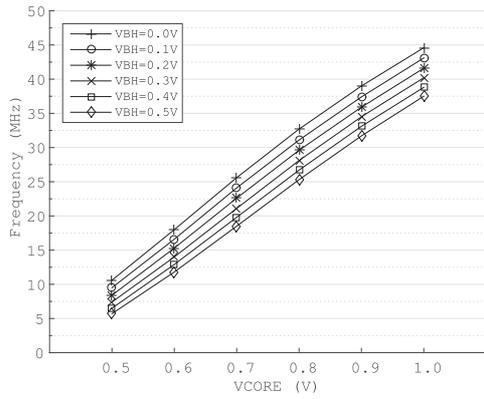


Fig. A-4 Max frequency of the ADD32 circuit with unified biasing.

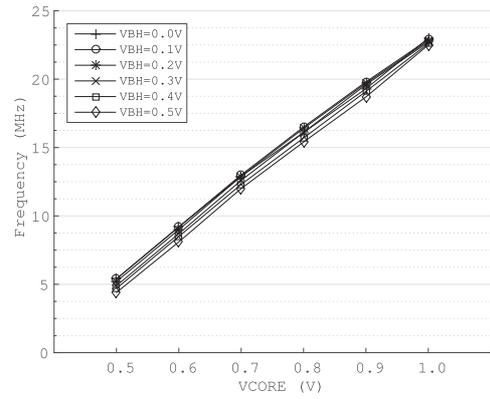


Fig. A-7 Max frequency of the MUL16 circuit with Flex Power.

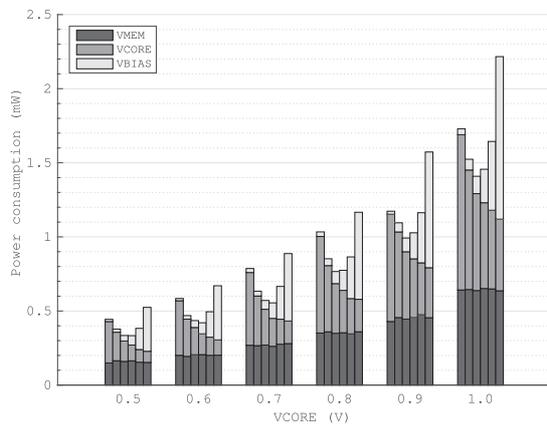


Fig. A-5 Static power of the MUL16 circuit with Flex Power.

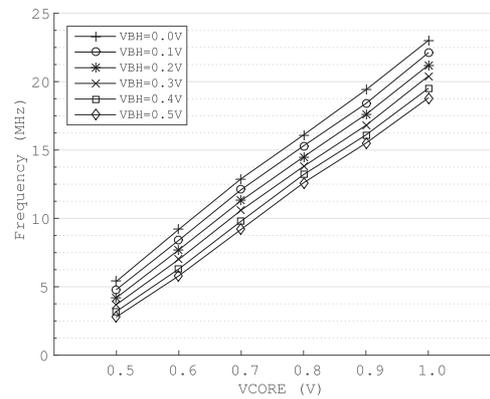


Fig. A-8 Max frequency of the MUL16 circuit with unified biasing.

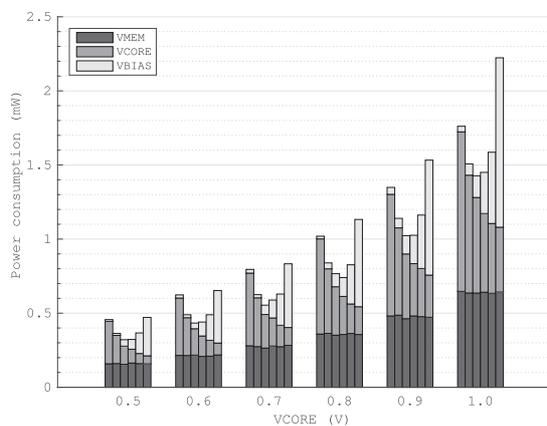


Fig. A-6 Static power of the MUL16 circuit with unified biasing.

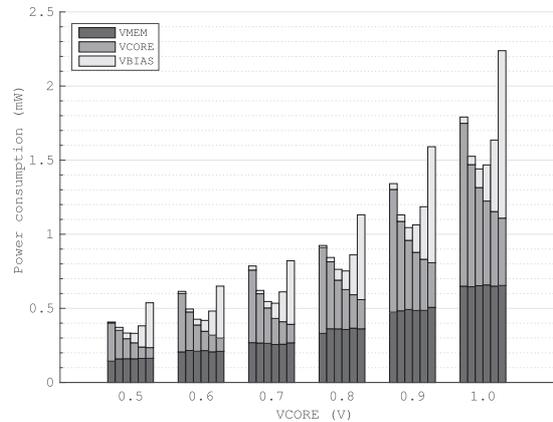


Fig. A-9 Static power of the SBOX circuit with Flex Power.

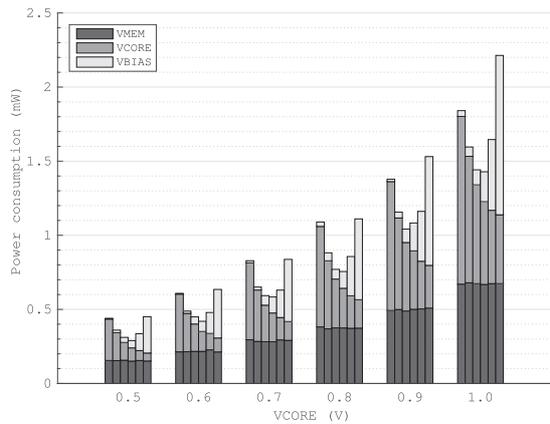


Fig. A-10 Static power of the SBOX circuit with unified biasing.

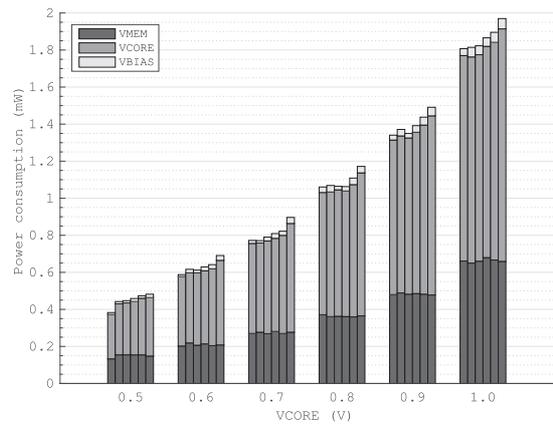


Fig. A-13 Static power of the ADD32 circuit with Flex Power.

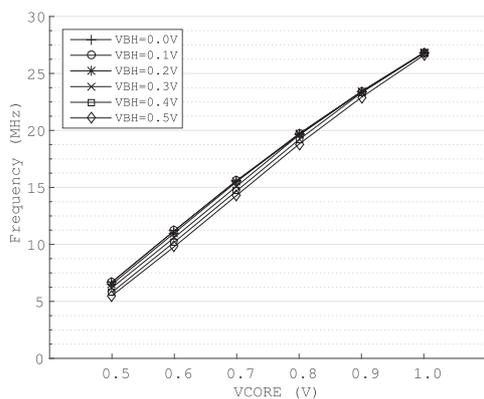


Fig. A-11 Max frequency of the SBOX circuit with Flex Power.

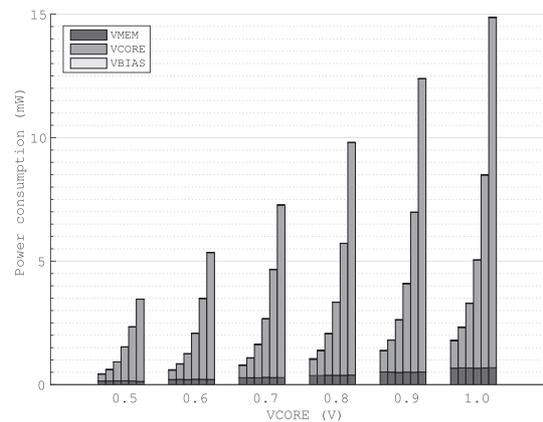


Fig. A-14 Static power of the ADD32 circuit with Unified biasing.

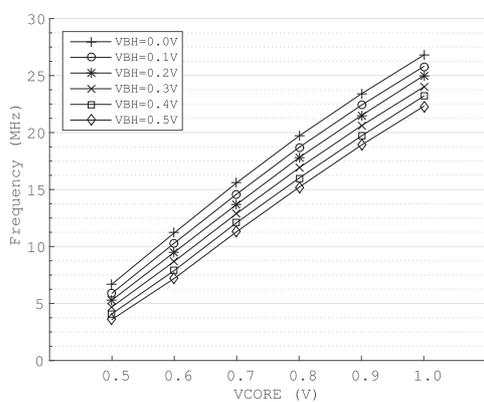


Fig. A-12 Max frequency of the SBOX circuit with unified biasing.

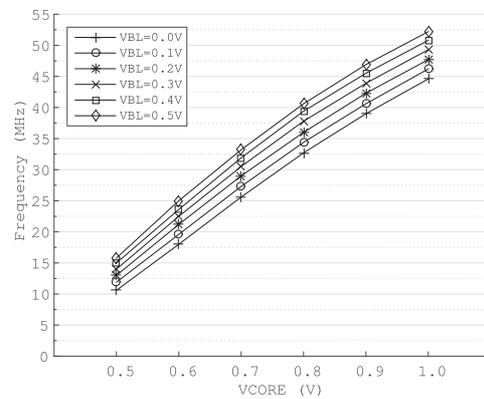


Fig. A-15 Max frequency of the ADD32 circuit with Flex Power.

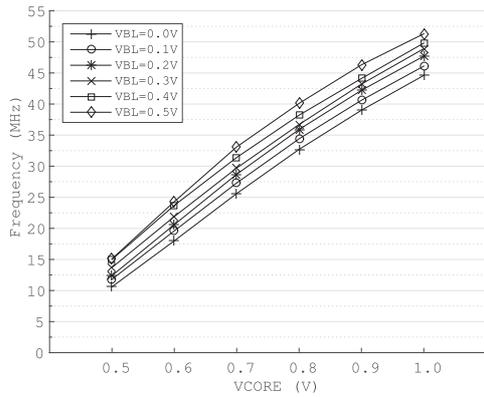


Fig. A-16 Max frequency of the ADD32 circuit with unified biasing.

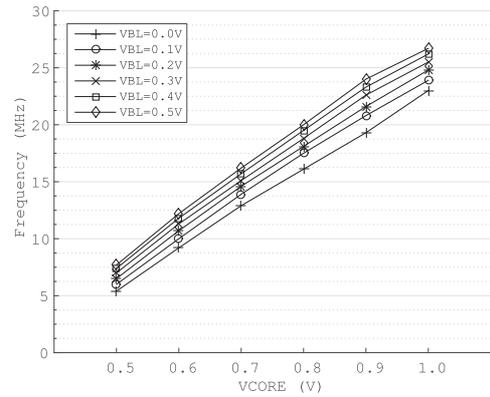


Fig. A-19 Max frequency of the MUL16 circuit with Flex Power.

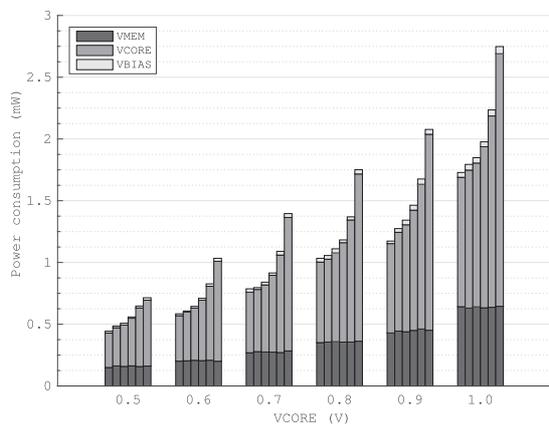


Fig. A-17 Static power of the MUL16 circuit with Flex Power.

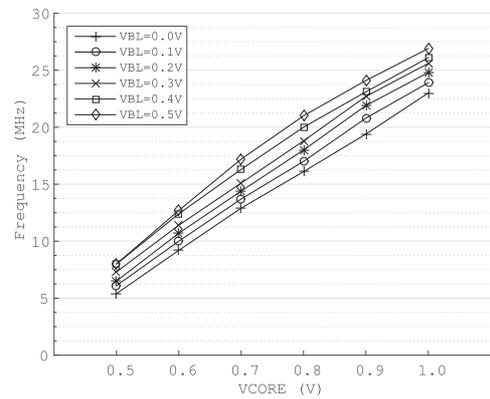


Fig. A-20 Max frequency of the MUL16 circuit with unified biasing.

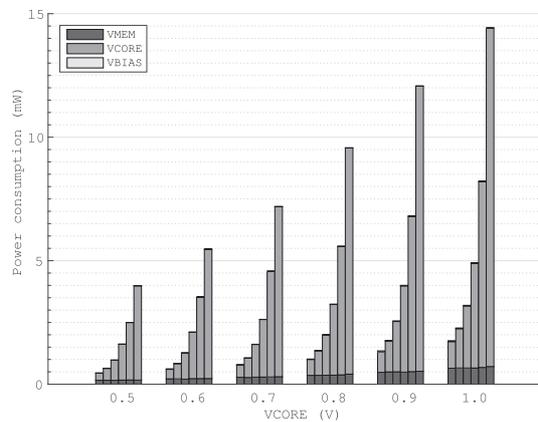


Fig. A-18 Static power of the MUL16 circuit with unified biasing.

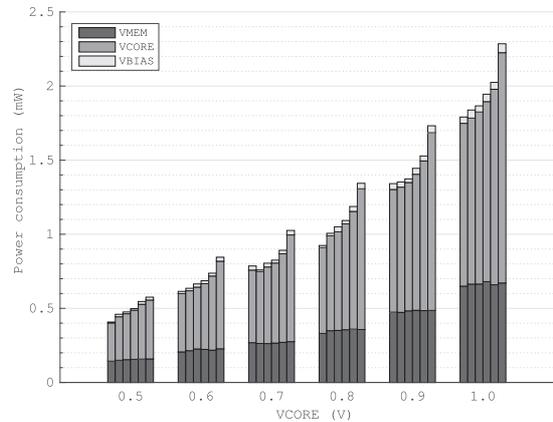


Fig. A-21 Static power of the SBOX circuit with Flex Power.

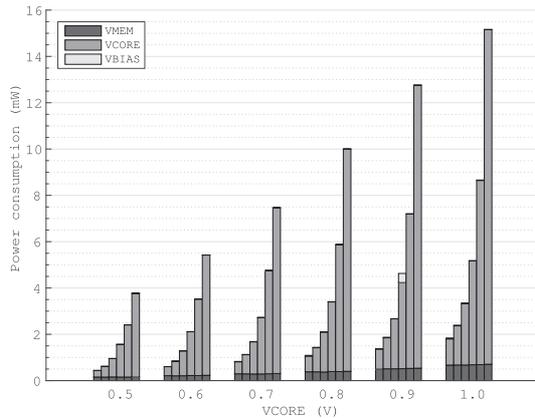


Fig. A-22 Static power of the SBOX circuit with unified biasing.

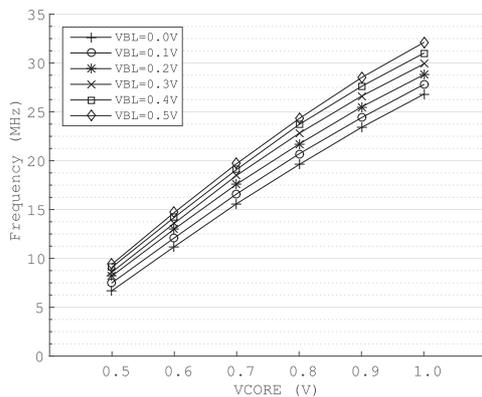


Fig. A-23 Max frequency of the SBOX circuit with Flex Power.

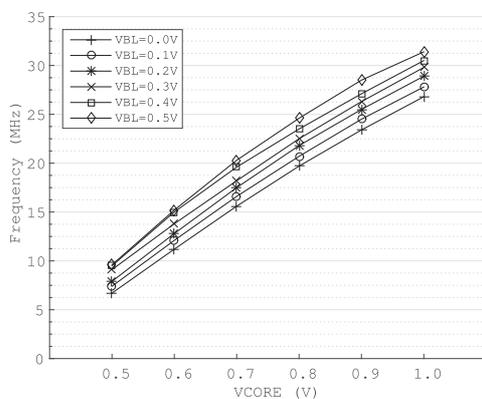


Fig. A-24 Max frequency of the SBOX circuit with unified biasing.



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